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DESIGN AND ANALYSIS OF EPS HOUSING AND CIRCUIT BOARDS FOR PANSAT

by

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DESIGN AND ANALYSIS OF EPS HOUSING AND CIRCUIT BOARDS FOR PANSAT

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Submitted in partial fulfillment
of the requirements for the degree of

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ABSTRACT

PANSAT, the Petite Amateur Navy Satellite, is a small spacecraft being built at the Naval Postgraduate School. The electrical power subsystem (EPS) contains two circuit boards which act as an interface between the EPS and other subsystems, receiving and distributing electrical power. This thesis covers the design and analysis of the housing for the two circuit boards and the circuit boards themselves. The structures were analyzed for strength and frequency response using classical methods and computer based finite element models (FEM). With the addition of a stiffener to decrease the deflection of the circuit boards during vibration all structures appear to meet launch load specifications in the Space Shuttle. The thesis concludes with a discussion of Electromagntic Interference (EMI) issues and how to deal with them.

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I. INTRODUCTION

A. PANSAT MISSION

PANSAT, the Petite Amateur Navy Satellite, shown in Figures 1 and 2, is a small satellite being constructed at the Naval Postgraduate School (NPS). It is a communications satellite which uses spread spectrum modulation with an operating center frequency of 436.5 MHz and is spread to a bandwidth of 2.5 MHz. The satellite operates on a store-and-forward basis, storing messages that it receives while passing overhead a ground station, and then downloading them to other ground stations as it passes over them. Its downlink uses a bit rate of 9600 bits per second and it has four Mega bytes of memory available for data storage. PANSAT will be used by students at NPS as well as other amateur radio users. It will be placed into a low earth orbit, and has a life expectancy of approximately two years. [Ref. 1]

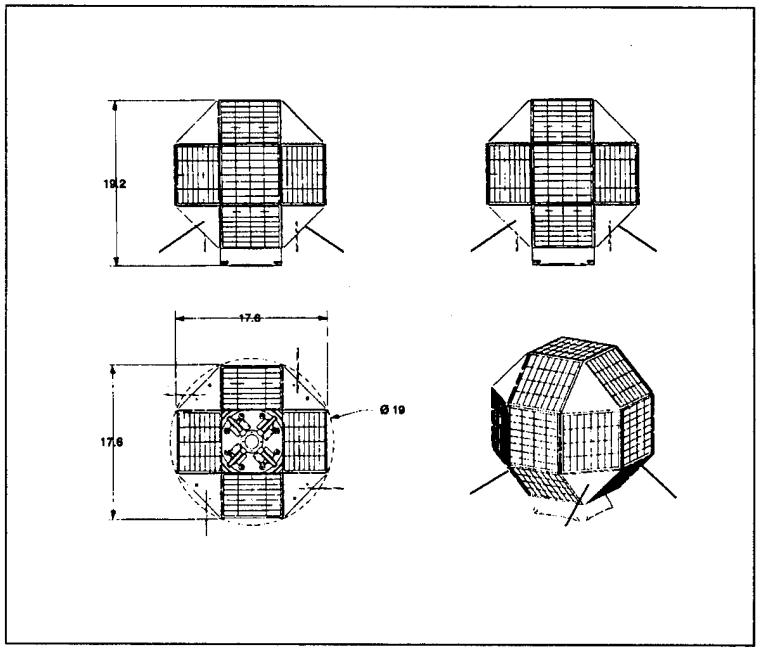


Figure 1. PANSAT Overall Dimension [Ref. 2]

The spacecraft is generally spherical in shape but is actually made of 18 small, square panels and 8 triangular panels so that it presents an octagonal (stop sign) profile from any view; front, back, top or bottom. The square panels measure 7.125 inches by 7.125 inches. It is designed to fit into a cylindrical payload envelope and is 19.2 inches in height and 17.6 inches in diameter. The primary structure is manufactured from 6061 T651 aluminum. The satellite does not have an attitude control system, but instead tumbles in orbit. Electrical power is provided by solar cells which cover the outer panels. Four dipole antennas are located on the bottom half of the spacecraft bus for communication. The entire satellite has a weight of 150 pounds.

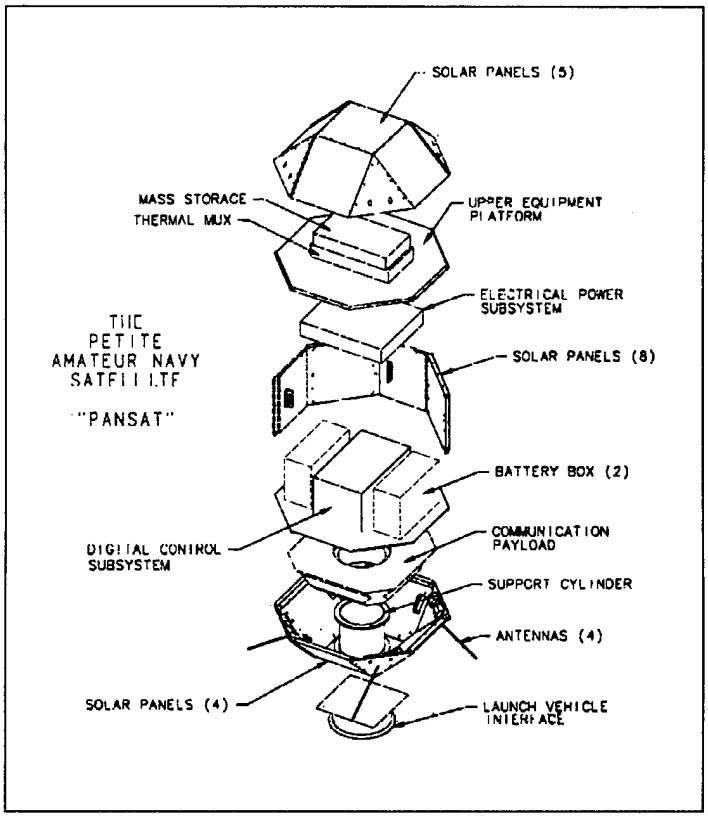


Figure 2. PANSAT Exploded View [Ref. 2]

There are two equipment plates which are used to support the various subsystems. The locations of the subsystems inside the satellite can be seen in Figure 2. These are also

manufactured from aluminum. These subsystems include communications, digital control, and electrical power. The electrical power subsystem (EPS) includes the solar cells, batteries, two circuit boards, and associated wiring. The EPS housing contains the two circuit boards and is mounted under the upper equipment plate. The housing and the circuit boards are the focus of this thesis. The following sections and chapters discuss their requirements, design and analysis.

B. LAUNCH VEHICLE

The housing and circuit boards must be designed so that they are robust enough to withstand the most severe loading conditions expected during flight. This worst case typically occurs during launch, when accelerations and vibrations produced can create high stress levels in the satellite. These loading conditions are a function of the launch vehicle selected for the mission.

PANSAT will be launched aboard the Space Shuttle, utilizing the Shuttle Hitchhiker program. The purpose of the program is to encourage the use of space by all researchers and is designed to allow relatively inexpensive access to space. Hitchhiker payloads are manifested on the shuttle on a space available basis, first-come, first-served. Since the payload is not a primary payload, it is required to accept the orbit to which the shuttle mission is designed.

While PANSAT is being designed with the shuttle in mind, the possibility of using a refurbished Minuteman ICBM is being examined as well.

1. Gas Can

Hitchhiker payloads are referred to as Get Away Special (GAS) Small Self Contained Payloads (SSCP). They are located in the shuttle payload bay inside small cylindrical canisters, hence the name GAS CAN. A GAS CAN is shown in Figure 3.

The GAS containers are made of aluminum. They have a usable volume of approximately 5.0 ft^3 . Allowable payload size is 19.75 inches in diameter and 28.25

inches in height, with a weight of up to 200 pounds. For ejectable payloads like PANSAT, the allowable mass is limited to 150 pounds and the allowable payload size is reduced to 19 inches by 20.5 inches. The container is sealed, and can be pressurized from a near vacuum up to one atmosphere. The exterior is thermally insulated on the sides and bottom, and the top may be insulated depending on the payload . The container isolates the payload from the Orbiter, and as a result is considered self contained. The payload is required to have its own electrical power, heating and data handling facilities within the GAS container. It is not allowed to use any of the Orbiter's own systems [Ref. 3].

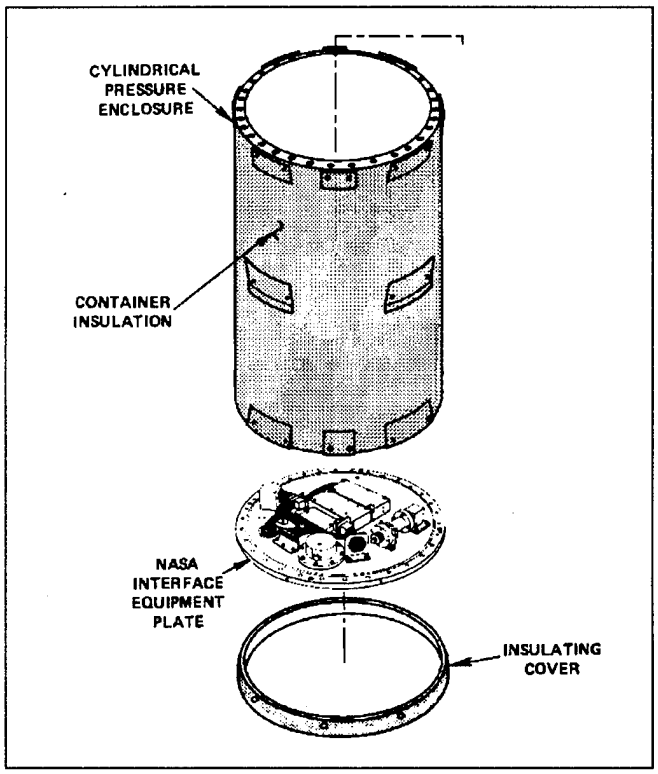


Figure 3. GAS CAN [Ref. 3]

2. Launch Loading

The worst case loading to the structure will occur during launch by the Shuttle. By comparison, separation from the GAS can will be accomplished using a Marmon clamp

mechanism with a separation velocity of 2-4 feet per second and is not considered significant.

The Space Shuttle requires stringent safety standards for all payloads transported into space via the Hitchhiker program. These factors include structural testing at 1.25 times the limit loads. Material failure such as fracture or buckling must not occur at less than 1.4 times the limit loads. The SSCP allows qualification by analysis alone, instead of actual testing, using a factor of safety of 2.0 times the limit loads for material yield and 2.6 times the limit loads for ultimate failure. This method is being used for PANSAT, however NASA reserves the right to require structural testing for complex structures. The limit loads for the Hitchhiker program are listed in Table 1.

Axis	Load Factor (g)	Angular Acceleration (rad/sec^2)
X	±11	±85
Y	±11	±85
Z	±11	±85

Table 1. Hitchhiker Payload Limit Loads

These limit loads encompass the worst possible launch environment. They include steady state, low frequency transient and higher frequency vibro-acoustic launch and landing loads. These values apply directly to the main structural members of PANSAT. For smaller, non-structural components and equipment inside the satellite, load factors which take into account the transmissibility between the payload's primary structure and the component are to be used. These values are used as input in determining the transmissibility. If the transmissibility cannot be measured or reasonably estimated then the component must be analyzed using a 40 g load in the most critical direction and a 12-g load (30% of the maximum) in the other two directions. This applies to components weighing less than 20 pounds. For PANSAT, the critical axis is its lateral axis. [Ref. 4]

A reasonable estimate of transmissibility is available for the EPS circuit boards, and they are analyzed accordingly. For the housing, the alternate loads outlined above are used.

The SSCP program requires that the natural frequency of all equipment be greater than 35 Hz. It is desired that it be above 50 Hz. It also requires a stress analysis which must be done in sufficient detail to show that the margins of safety are met. The following equation is used for margin of safety.

$$MS = \frac{allowable\ stress}{(\text{safety factor})(\text{actual stress})} - 1 \geq 0 \qquad (1.1)$$

where MS = margin of safety.

II. EPS OVERVIEW

The PANSAT EPS is responsible for receiving and distributing electrical power generated by the solar cells and batteries. Figure 4 is a block diagram of the EPS, showing the paths for power flow to and from the logic and switch (power) boards. It also indicates which systems are using the power. These two boards are the key to the EPS. A smaller mother board located at the rear of the EPS housing provides a link between the two. The boards are made of polyimide and each weighs approximately 0.31 pounds. They are supported structurally by the EPS housing. A brief overview of the boards and the housing follows here.

A. EPS CIRCUIT BOARDS

Figures 5 and 6 show the "foot prints" of the switch and logic boards. These figures show the locations of the various components mounted to each board as of 1 May 1995. Minor modifications were being considered which may change the board layout.

The primary functions of the switch board are to control power distribution to the spacecraft bus subsystems, place the batteries in a charging or discharging state, and bring the batteries on or off line. This is accomplished with switches. Each switch is made up of P-channel (positive) and N-channel (negative) MOSFETs (metal oxide semi-conductor field effect transistors). The P-channel MOSFETs are depicted by the large gasket like objects on the circuit board footprint. A logic one, which is a high voltage signal, turns on the N-channel MOSFET while a logic zero turns on the P-channel MOSFET. By turning switches on and off the flow of power is controlled. [Ref. 5]

The components on the board have a weight of approximately 0.44 pounds which give the board a total weight of approximately 0.75 pounds.

The logic board performs several functions. It can be divided into four sections. The top right section contains 11 current sensors. This includes one for the spacecraft power bus, eight for the roll rate experiment, which are tied directly to solar panels, and

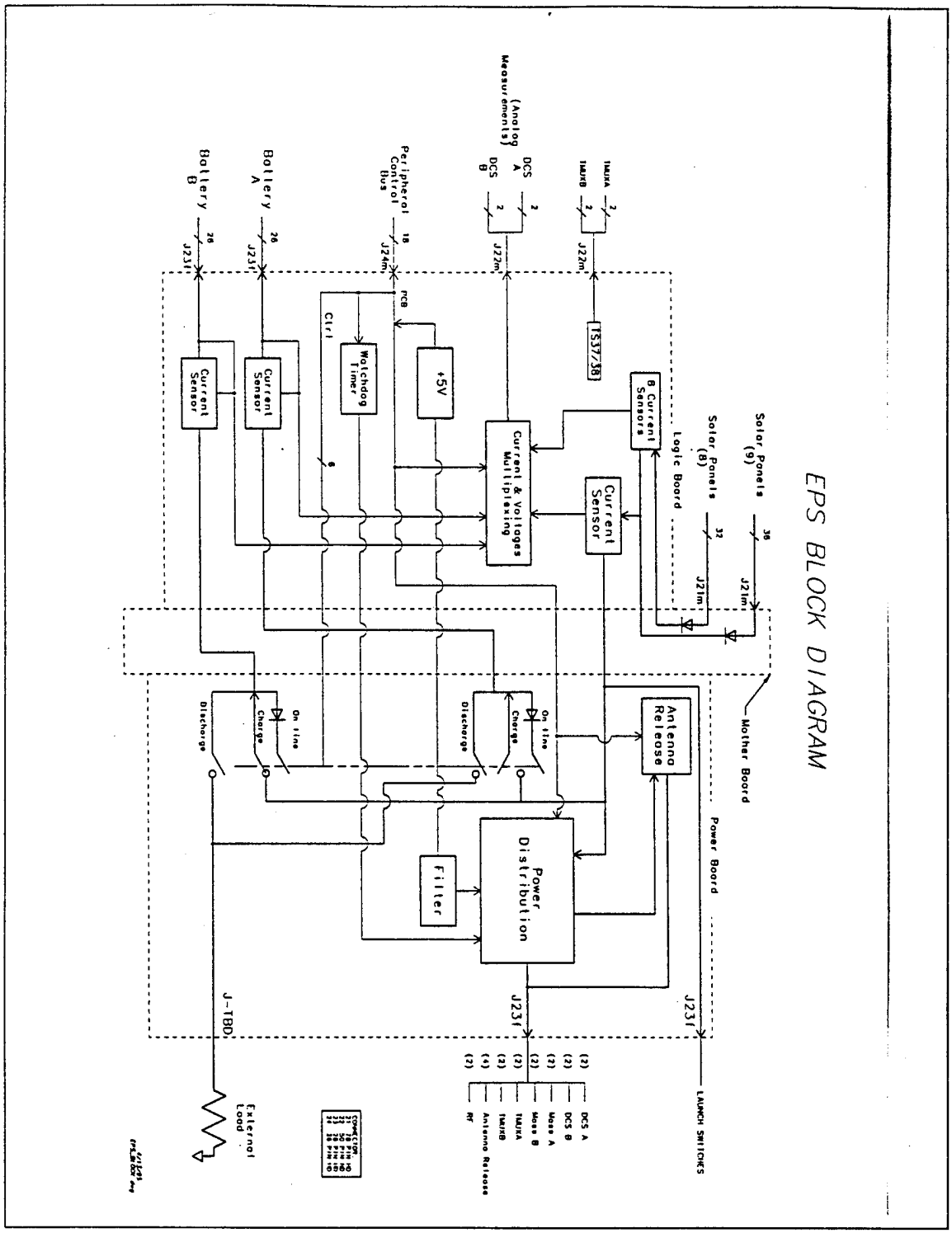


Figure 4. EPS Block Diagram

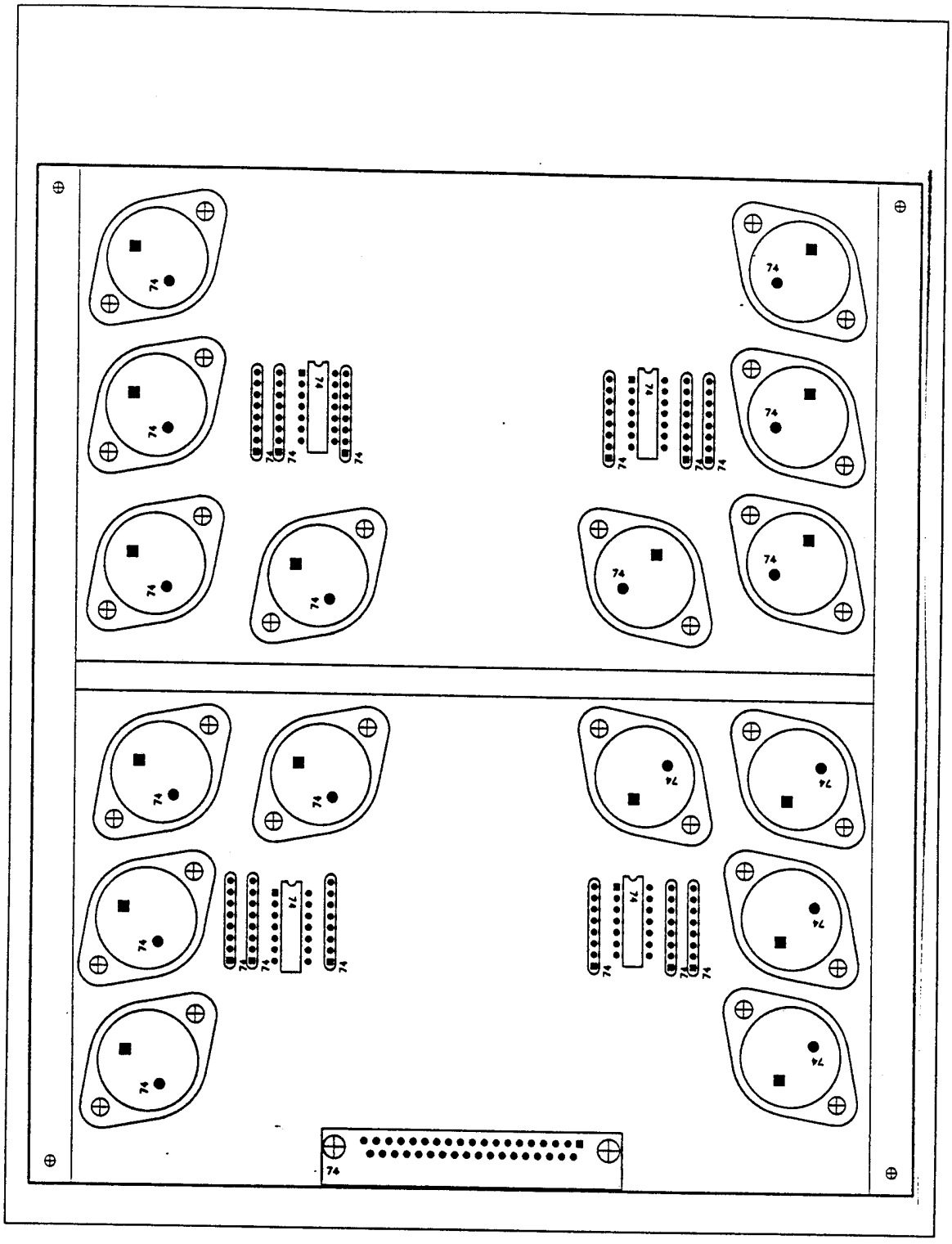


Figure 5. Switch Board

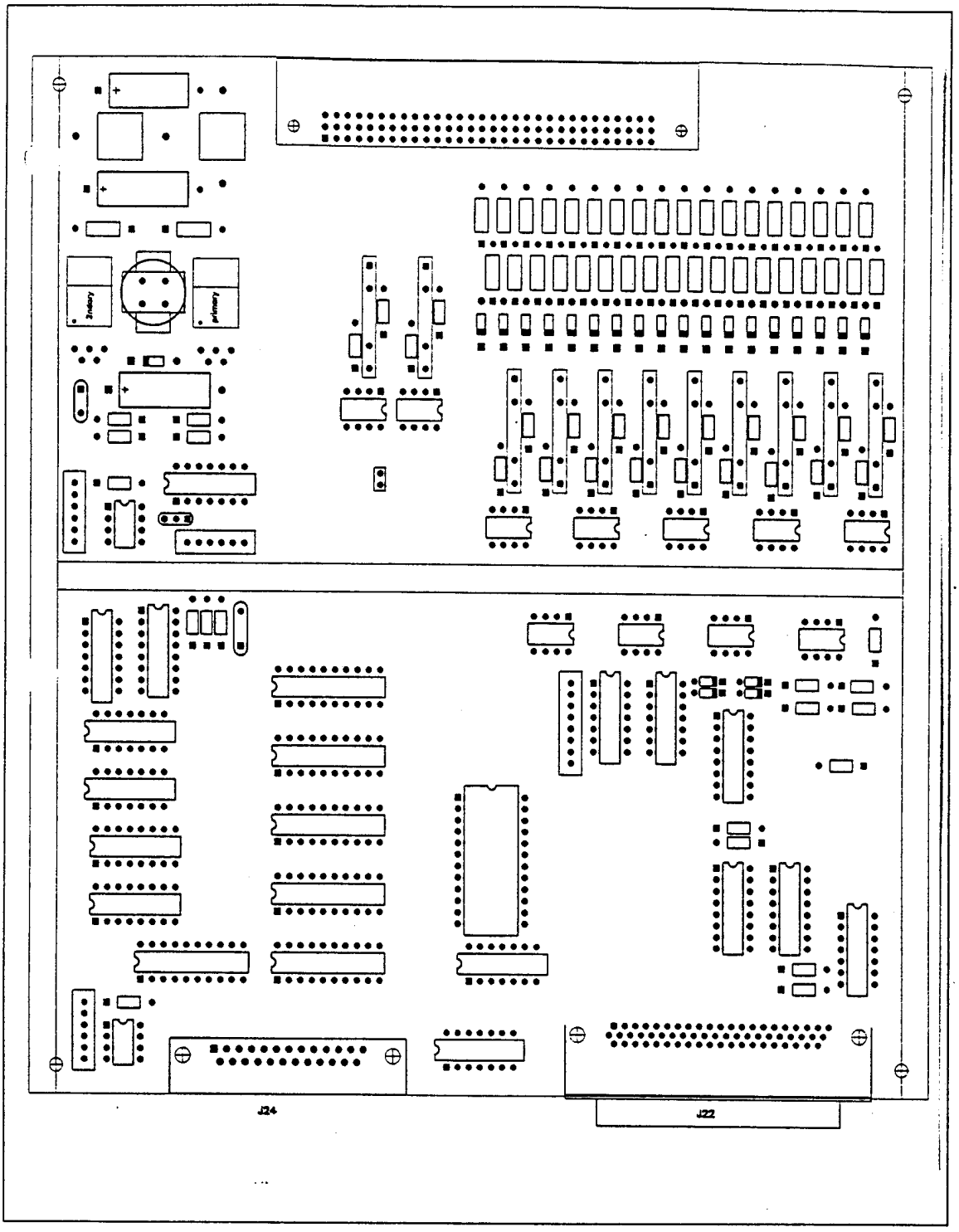


Figure 6. Logic Board

two for battery charge and discharge . The bottom right quadrant contains the circuitry for the multiplexing of the battery cell voltage, spacecraft power bus voltage and current sensors. The bottom left section has the Peripheral Control Bus interface. It controls the multiplexing circuitry located on the bottom right quadrant, and the switching on the switch board. The upper left quadrant has the watch dog timer and the DC-DC converter which converts 15 volt spacecraft voltage to 5 volts for use by the logic board. Specific details about these components and their exact operation can be found in the PANSAT reference.

The approximate weight of the components on the logic board is 0.23 pounds. This makes the total for the logic board 0.54 pounds.

Most of the circuitry on the boards is analog. The switch board is all analog. The logic board is analog except for the bottom left section which uses digital logic.

The circuit boards are multilayered and two sided. The printed circuitry makes up the top and bottom layers, and is why the board is considered two sided. In between these two layers are power and ground layers made of copper, and three layers of polyimide which separates each of the four layers mentioned.

The circuit boards, which are inside the housing, must communicate with the spacecraft subsystems outside the housing. To accomplish this, D-connecters are used to carry the wiring of the subsystems through the housing walls to join with the circuit boards. The switch board has one D-connector at the front of the housing. The logic board has two. Their locations on the circuit boards are shown in Figures 5 and 6. Figure 7 shows a D-connector.

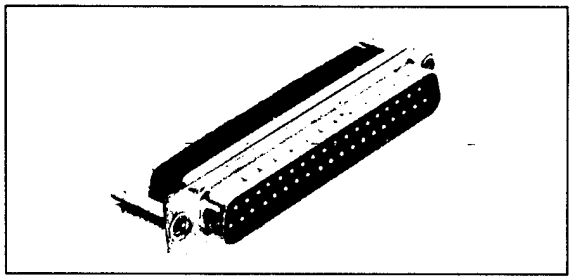


Figure 7. D-connector

To attach the circuit boards to the housing, Calmark Corp. card-loks are used. A card-lok is shown in Figure 8. These card-loks are mounted to the boards and then the assembly is placed into the housing, resting on gaps cut into the side walls. They are made up of several wedge shaped pieces with a bolt running through the center. The center wedge is fixed to the circuit board, while the outer wedges are free to move. As the bolt is tightened, the free moving wedges move toward the center wedge, sliding up its edge so that the height increases. This increase in height clamps the circuit board to the housing.

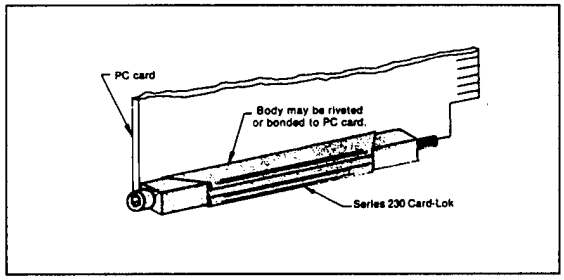


Figure 8. Card-lok

Detailed figures of the D-connectors and card-loks, including their dimensions are contained in Appendix A.

B. EPS HOUSING

The EPS housing serves primarily as a structural support for the circuit boards and is made of four pieces of aluminum: the top, front and back covers, and the sides and bottom which are made from one piece of aluminum. An exploded view of the housing is shown in Figure 9. Additionally it serves as a thermal path and an EMI protection shield. The housing is basically a hollow aluminum box measuring 2.05 x 8.30 x 10.00 inches. These dimensions are determined mostly by the size of the circuit boards and the available volume with which to work inside the satellite body. A 0.40 inch flange has been added to the sides, so that the housing extends 9.10 inches at the top. This flange is used to attach the housing to the upper equipment plate.

The circuit boards are placed inside the housing so that they are 'back-to-back'. The switch board is facing down and the logic board is facing up. To support the circuit boards two gaps have been removed from the right and left walls. The gap size depends on the size of the particular card-lok chosen. Series 230 card-loks were selected for the EPS. There is 0.25 inches between the two boards and 0.775 inches between the boards and the top and bottom of the housing. The housing is 1/16 inch thick on the top and bottom and 0.425 inches thick on the sides, excluding the card-lok gaps. The sides do not need to be this wide from a strength perspective, but the extra thickness provides an area to place the screws that are used to fasten the housing together. A more detailed discussion follows in Chapter VI.

The circuit boards generate approximately two watts of thermal energy at 15 volts. This energy is radiated and conducted away from the board. The housing will capture the radiated energy and conduct it away form the circuit boards. The card-loks provide a tight interface between the boards and the housing, which creates a thermal path for heat to conduct away from the circuit boards and the housing.

Room for a groove has been provided in the top of the housing to allow the placement of an EMI gasket. The design does not show the groove since the specific gasket has not been selected. Other EMI reduction techniques have been included also. These are discussed in more detail in the EMI section of Chapter VI.

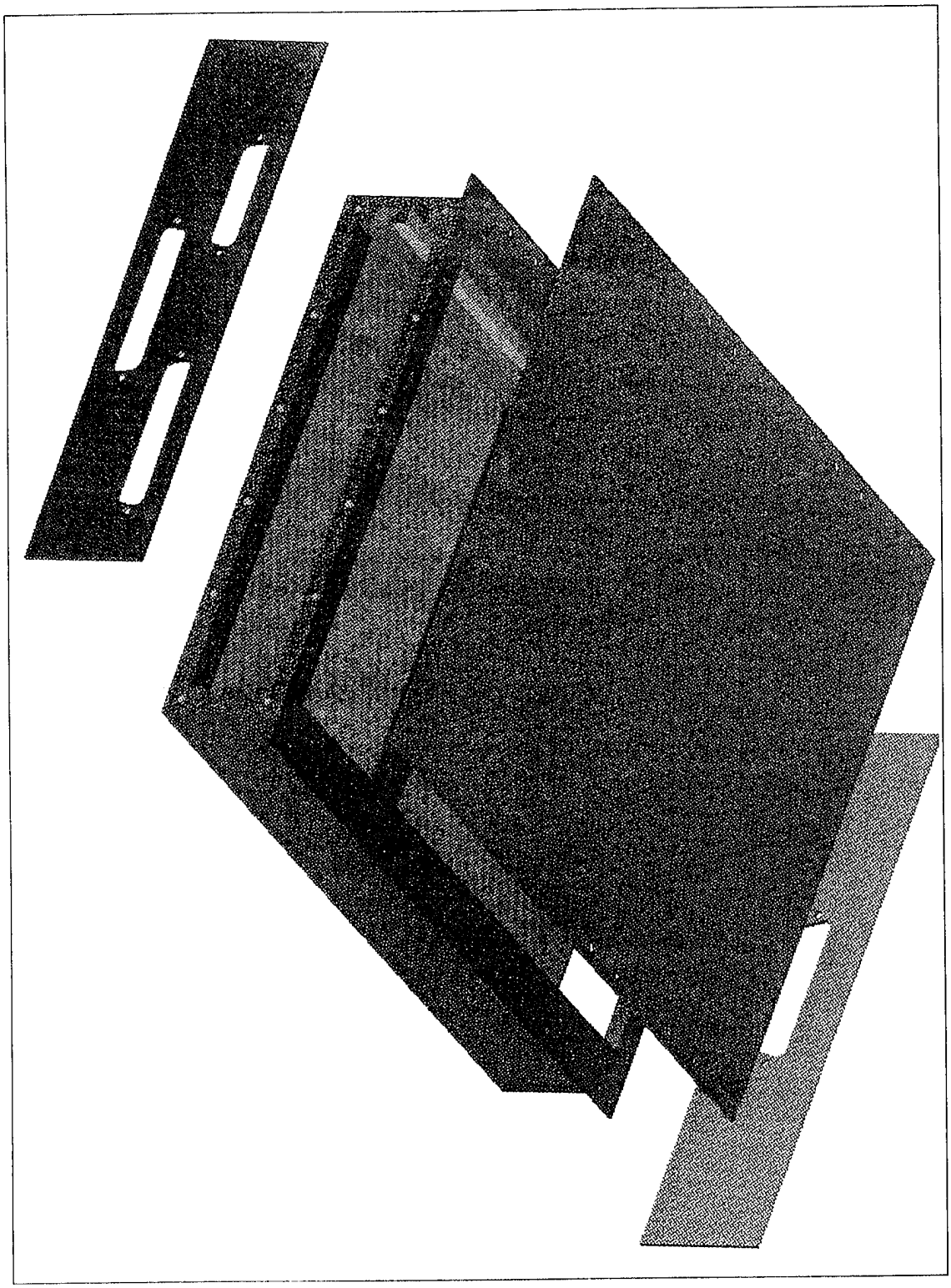


Figure 9. EPS Housing

III. FINITE ELEMENT THEORY

With structures more complicated than simple beams or plates, it is difficult to apply classical methods to solve for stresses and strains. Beam and plate theory are idealizations which use certain simplifying assumptions which are not valid for more complex structures. These structures often have discontinuities such as cutouts for screws which make the traditional analysis less accurate. Additionally, these structures are usually statically indeterminate. This makes exact solutions using the governing differential equations very impractical. Finite element theory was developed to solve these kinds of problems. Finite element theory handles the problem by analyzing the entire structure as though it were made up of several smaller elements. These elements are usually very simple and are easily analyzed. Finite element theory is used to analyze the EPS circuit boards and housing.

A. MINIMUM POTENTIAL ENERGY

A deformable body under external loading will develop internal stresses and come to a point of equilibrium [Ref. 6]. The Principle of Minimum Potential Energy can be used to develop equilibrium equations. The governing equation is

$$\Pi = U + V \tag{3.1}$$

where

Π = Total Potential Energy

U = internal, or strain energy potential

V = external potential energy

The external potential energy, V, can be divided into two terms. One term if due to applied distributed loads, such as gravity. The other is due to applied point loads. These applied point loads cause deflections which vary from node to node and are transmitted from one element to the other.

The form for the strain energy equation depends on the type of element chosen for the finite element model. Several different elements exist. The shape of the structure usually points to the use of a particular element. These elements include beam elements, thin shell elements, triangular elements, and others. They will be discussed more later. The equilibrium equation follows

$$[K]\{q\} = \{Q\} \tag{3.2}$$

where

{K} is the stiffness matrix

{Q} is the force matrix

{q} is the deflection matrix.

The stiffness matrix, {K}, is given by

$$K_{ij} = \frac{\partial^2 U}{\partial q_i \partial q_j} \tag{3.3}$$

where the indices i and j correspond to the number of nodes in the structure and the degrees of freedom for each. An object with three elements and three degrees of freedom for the nodes which connect them will have a stiffness matrix that is 9 x 9. U, strain energy, will be given by the element type.

{Q} is given by

$$Qi = -\frac{\partial V}{\partial q_i} \tag{3.4}$$

The deflection at each node is represented by {q}. The vector {q} is a column vector whose dimension is determined by the number of nodes in the finite element model and the number of degrees of freedom for each. For example, an object with three nodes that each have two degrees of freedom would have a {q} vector with six elements.

{Q} can be broken into two parts to correspond to the two different sources of V. The potential energy created by applied distributed loads is represented by {F} while the

contribution due to applied point loads is given the symbol {S}. They are also column vectors with the same dimension as {q}. Equation (3.2) can be written

$$[K]\{q\} = \{F\} + \{S\} \tag{3.5}$$

To solve the finite element model, the boundary conditions that exist must be considered. These provide the needed data to solve for {q}, and {S}.

B. TYPES OF ELEMENTS

The structure being analyzed will determine what element type is the best choice. The state of stress that exists in the body must be considered. Objects which are thin and under plane stress only can be modeled by thin shell elements. Objects which are larger and have a three dimensional stress state can be modeled with solid "brick" elements.

Large objects with many nodes can have very large stiffness matrices. The calculation problem can quickly become cumbersome. The process is straightforward, however, and lends itself easily to computer generated solutions.

IV. I-DEAS

The analysis of the EPS housing and circuit boards was done on I-DEAS™ Master Series 2.0 software. This is a computer aided design software produced by Structural Dynamics Research Corporation (SDRC) of Milford, Ohio [Ref. 7].

I-DEAS was used to generate finite element models (FEM). A finite element model is the complete idealization of the entire structural problem. This includes node locations, elements, physical and material properties like thickness and material type, loads and boundary conditions.

I-DEAS produces FEMs in three steps. They are pre-processing, solution, and post-processing. Pre-processing involves creating the geometry of the object, entering physical (how big is it) and material (what is it made of) properties and adding boundary conditions. The defined model is solved in the solution step. Several types of solutions are available such as linear static, normal mode dynamic and buckling analysis. The desired type is selected in the pre-processing step, and used in the solution step. In the post-processing step the results are displayed. There are several options to choose from when displaying the data, based on what the user is trying to determine with the model. Some examples are stress, strain and deformation.

The pre-processing step is broken down further into basic tasks. These include Master Modeler, Meshing and Boundary Conditions. The model geometry is defined in the Master Modeler Task. Here the user creates the object for which the FEM will be made.

In the Meshing Task the actual nodes and elements are generated. The software allows the structure geometry to be used to generate the mesh easily. Several types of elements can be selected, based on the geometry. These include linear elements which only have two nodes along each edge, parabolic elements which have three and cubic elements which have four nodes along each edge.

Depending on the object, it may be possible to choose from two basic meshing types: free or mapped. Mapped meshing requires that the same number of elements be on opposite sides of the mesh area and the mesh area must be bounded by three or four edges. [Ref. 7] The circuit boards are an example of an object which uses mapped meshing. The housing has several edges which make a mapped mesh impractical. Any object can be free meshing. This option only requires the user to select the element size, or to use the default length if acceptable. Once the mesh is created the user has the option of accepting it or changing some of the parameters and performing a remesh until it is acceptable. Figures 10 and 11 show the logic board and the housing after they were meshed. The logic board is mapped meshed using thin shell linear elements for the circuit board and solid linear elements for the stiffener. The housing is a free mesh using solid linear elements.

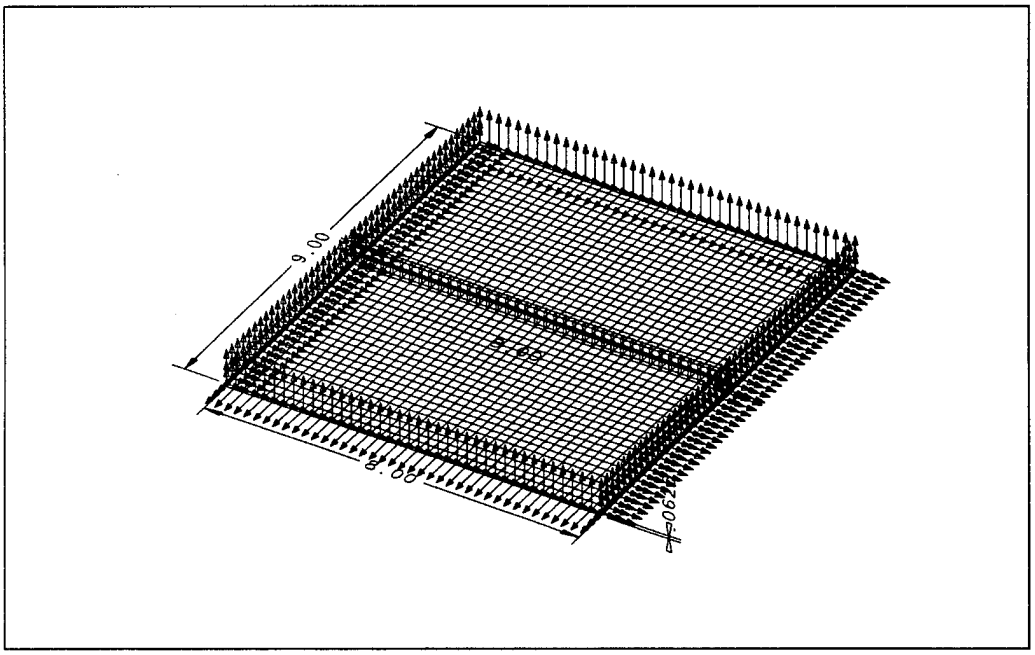


Figure 10. Meshed Logic Board

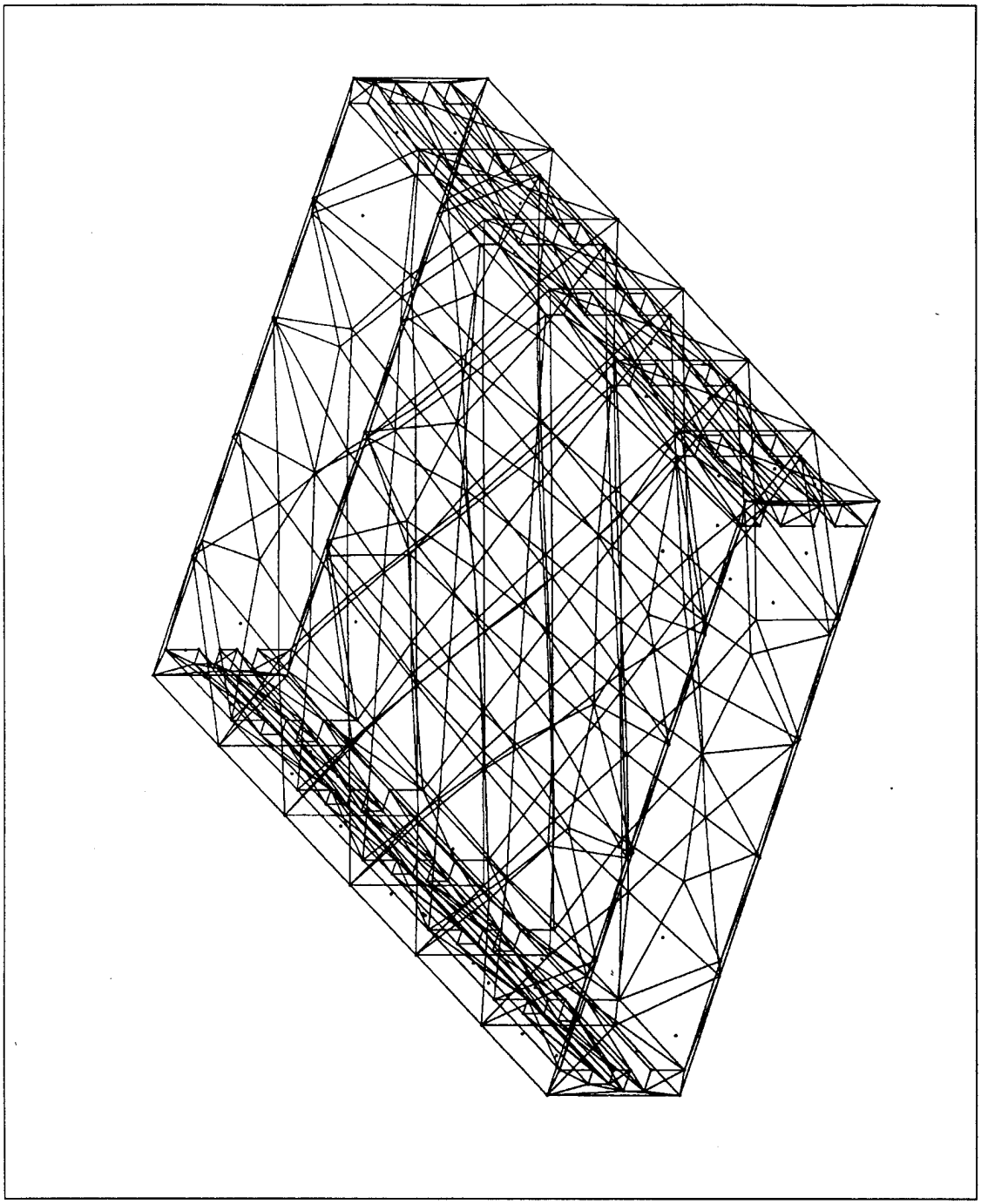


Figure 11. Meshed EPS Housing

The type of mesh, free or mapped, used for solid elements can have a critical impact on the model solution. Mapped meshing uses elements which are cube shaped. Free mapping uses tetrahedral elements. Great care must be given to the size of the elements chosen when using tetrahedral elements. Typically the default value presented will create elements which are much too large. The size of these elements must be selected so that it is no larger than the smallest dimension of the object being meshed. For example, the smallest dimension of the EPS housing is the 1/16 inch thickness of the walls. However, since the sides of the walls are 8.25 inches by 10 inches, the default value for the size of the tetrahedral elements is much larger than 1/16 inches. If this value is used the solution will be incorrect The mesh shown in Figure 11 has elements which are too big. Because of the erroneous results this model was not used. This is discussed in more detail in Chapter VI.

Once the mesh has been created, boundary conditions must be applied. Boundary conditions provide key information which will be used to reduce the number of knowns and unknowns in the solution of the model. The arrows in Figure 10 indicate the boundary conditions, and in this example represent sides which are pinned.

In I-DEAS boundary conditions may be applied directly to the nodes or to the object geometry . Applying them to the geometry allows the boundary conditions to be updated if the part is changed. Boundary conditions include forces acting on the object, thermal loads, pressures, geometric constraints, gravity, etc. These are all placed into a Boundary Condition Set in I-DEAS. A large potential for error exists at this point. It is important that the boundary conditions be chosen very carefully. Incorrect boundary conditions will lead to discontinuities in the solution, and perhaps prevent the solver from converging to an answer.

In the solution step I-DEAS creates a solution set in which it places the Boundary Condition Set. The user also selects the desired output, such as stress, strain and frequency. These items are also placed into the solution set. The user can create several

different solution sets and then pick and choose between them. Once these items have been selected the model is solved.

I-DEAS can perform several types of solutions, including statics, buckling, heat transfer, potential flow and dynamics. The EPS was analyzed using a statics solution and a dynamics solution. The statics solution was used to determine stress and deflection due to launch loads. The dynamics solution was used to determine resonant frequencies.

For the statics solution the possible outputs include displacement, stress, reaction forces and strain energy. Both the EPS housing and circuit board FEMs were solved using a static solution, with displacement, stress and strain as the desired outputs.

The EPS housing and circuit boards were also solved using a dynamics solution. In this case the selected outputs were mode shapes and mode frequencies. The user may also select the number of modes to be determined. The first three modes were generated in this case.

In Post-processing the user selects how the results are displayed. Several options are available. A contour map can be created which shows the various levels of stress or deflection in the model. The deformed model can be displayed with the undeformed model to show the degrees of deflection. Graphs can be created, specific elements can be probed and the model can be animated as well. For the EPS I-DEAS was used to display stress, displacement and mode shapes.

V. EPS CIRCUIT BOARDS

The EPS circuit boards are populated with several components responsible for controlling spacecraft power, as discussed in Chapter II. Electrical lead wires connect the components to the board. These wires are very thin and if broken will disrupt the flow of power, possibly causing spacecraft failure. The intense loads placed on the satellite during the launch environment will cause the circuit boards to vibrate, producing bending stresses in the electrical leads. If these stresses are high enough, the wires will break [Ref. 8].

Whether or not the wires break is a function of several factors, including board weight, component size, launch loads, how and where the components are mounted to the board, how long the vibrations last, what type of strain relief the lead wires have and the natural frequency of the board. This report examines primarily the effect of natural frequency, since these factors all have their most severe effect during resonant conditions.

The deflection for a rectangular plate supported on its edges increases from zero at the edges to a maximum at the center of the board. As the deflection increases the bending stresses will also increase. The stresses produced will also depend on the dimensions of the board. If the board is square, this is not relevant. If the board is rectangular, the stresses will be more severe when the component body is parallel to the short side of the board. Since the side is shorter, the change in curvature is more rapid. For this reason, rectangular shaped components are ideally placed so that the longer side of the component body is parallel with the longer side of the circuit board. Large components which are likely to experience differing stresses on varying parts of it are ideally located away from the center of the board so that the deflections (and stresses) are minimized. From Figures 5 and 6 of the logic and switch boards it can be seen that where feasible the components have been placed so as to minimize stresses.

The logic and switch board are analyzed using classical hand calculation methods and more sophisticated computer methods, using I-DEAS design software.

A. EXPERIMENTAL DETERMINATION OF POLYIMIDE PROPERTIES

For the analysis of the circuit boards the material properties of polyimide were required. Polyimide comes in several different compositions. To determine the properties of the particular polyimide composition used in PANSAT a sample of the material was taken to determine its density, modulus of elasticity (E) and Poisson's ratio (ν) experimentally.

Two sections were cut from the circuit board material. Each was cut roughly in the shape of a "dog bone". Figure 12 shows a sample. The large ends were used to provide a grip area for the Model 810 Universal Testing Machine used in the experiment. The narrow center region of the sample was the test section. The corners were filleted to prevent stress concentrations.

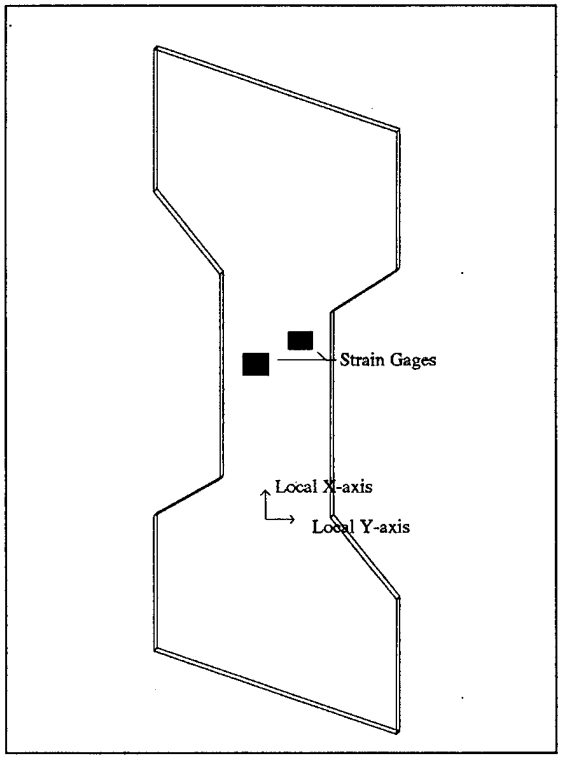


Figure 12. Circuit Board Test Sample

Two strain gages were placed in the test section area. The strain gages only measured strain in one direction, so one was aligned with the sample axial axis (local X)

and one was aligned along its transverse axis (local Y). The samples were pulled in tension and values for strain in both directions were recorded at various loading levels, until failure occurred.

Modulus of Elasticity, (E), relates stress and strain in a material. Stress was calculated from the applied load and cross sectional area and was plotted against strain along the local X axis. The slope of this plot is E. Poisson's ratio,ν, relates elongation in one axis due to elongation in another axis. This value was obtained by plotting strain in the X direction vs. strain in the Y direction where the slope of the curve is ν. The board was weighed and its volume calculated to determine density.

The results from each sample were slightly different. They were averaged to determine the values used in the analysis. Table 2 contains the averaged results. The experimental data, including the plots, can be found in Appendix B.

E (psi)	Poisson	Density (lb/in^3)
2.33×10^6	1.2×10^{-1}	6.48×10^{-2}

Table 2. Experimental Results

B. CLASSICAL ANALYSIS

The classical method of determining deflection was done two ways. One method relates deflection to the distributed load applied to the board and the board stiffness factor [Ref. 9]. The second method relates deflection to the resonant frequency of the board and the G forces acting on it [Ref. 8 p 30-31].

The relationship for the first method is given by

$$\nabla^4 w = \frac{q}{D} \tag{5.1}$$

where

∇ is the del operator

w = deflection

q = distributed load

D = plate stiffness factor

Deflection, w, is approximated by a double sine series, which is solved using Fourier analysis. The approximation depends on the boundary conditions applied. All four sides simply supported were used for the boundary conditions in this calculation. The equation follows: [Ref. 8]

$$w(x,y)=\Sigma\Sigma \frac{16q_o}{Dmn\pi^2\left[\left(\frac{n\pi}{b}\right)^2+\left(\frac{m\pi}{a}\right)^2\right]^2}\sin\left(\frac{m\pi x}{a}\right)\sin\left(\frac{n\pi y}{b}\right) \qquad (5.2)$$

A MATLAB program was used to solve the equation. The program and the details of the derivation can be found in Appendix C. The deflection results are discussed in section two of this chapter.

For the second relationship deflection at the center of the board is given by

$$\delta_r = 9.8 * G_{in} * Q/f_n^2 \qquad (5.3)$$

where

δ_r = deflection (in inches)

G_{in} = peak input acceleration

$Q = K\sqrt{f_n}$ = transmissibility

f_n = natural frequency [Ref. 8]

Q is related to the square root of the natural frequency of the board. The term 'K' in the equation above for Q represents this relationship. K generally varies between 0.5 and 2.0. The value for transmissibility, Q, is approximated, since an exact value for K is difficult to come by without actual test data on the design under consideration. An approximate value is needed in the design phase to determine if the design is acceptable.

Several factors influence Q. These deal mostly with the damping characteristics of the board, which determine how much energy is lost during vibration. When energy loss is high, not much energy is left to influence transmissibility and dynamic loads and stresses are lower. Higher deflection means higher energy losses. A trade-off develops

between having low deflection and energy loss. High deflection means high energy loss and low transmissibility, but high bending stresses which could cause the lead wires to break. Low deflection means not much energy is dissipated and the transmissibility is higher, but the bending stresses are lower. Equation (5.3) must be analyzed to determine which combination gives the lowest deflection.

The input acceleration force, G_{in} , also affects Q. A high acceleration force causes larger displacements which lowers Q. The type of edge support for the circuit board will also have an affect. A tight edge support, such as a clamp, will dissipate energy better and reduce Q. Circuit board connectors used for input/output wires also create damping effects which causes energy dissipation and lowers Q.

The circuit boards here are held into place via card-loks, which approximate a clamped edge. There are also D-connectors at both ends of the EPS housing. These factors tend to reduce Q. However, the shuttle G forces are very high, which tends to increase Q. In this report a value of 1.0 was chosen for K, since the design incorporates factors which tend to both increase and decrease K and 1.0 is a mid-range value.

1. Natural Frequency

To use the second method for determining deflection, the natural frequency of the circuit board is required. This can be approximated using the Rayleigh method with a trigonometric series or a polynomial series [Ref. 8]. In this report the trigonometric series was used.

In attempting to determine frequency, general plate equations are used to formulate equations for strain energy and kinetic energy of the vibrating plate. This produces an equation for natural frequency.

To use the Rayleigh method, a deflection curve is assumed which satisfies the given boundary conditions, which are deflection and slope at the edges. This assumed deflection curve is used to determine strain energy and kinetic energy. The frequency that is calculated will be a little higher than the actual value, unless the exact deflection curve is used.

The EPS circuit boards were analyzed using two boundary condition sets. One boundary condition was all four edges simply supported. The other was two sides simply supported plus two sides clamped. As mentioned, the card-loks clamp the sides and the connectors coming in the EPS housing to the circuit boards simply support the front and back edges. From the discussion on transmissibility, Q, the clamped edges will provide additional damping, which will increase the energy dissipation and decrease Q. The four sides simply supported case then serves as a lower limit in the design process.

For a simply supported plate, the deflection curve is represented by a double trigonometric series, summed for odd integers over m and n.

$$Z=\Sigma\Sigma A_{mn}\sin\frac{m\pi X}{a}\sin\frac{n\pi Y}{b} \tag{5.4}$$

where

Z = deflection

a, b = board length and width

The boundary conditions require no deflection at the edges, maximum deflection at the center, no slope at the center, some finite slope at the edges. Using these boundary conditions, the equations for total strain energy (V) and total kinetic energy (T) can be represented [Ref. 8].

$$V=\frac{D}{2}\int_0^a\int_0^b\left[\left(\frac{\partial^2 Z}{\partial X^2}\right)^2+\left(\frac{\partial^2 Z}{\partial Y^2}\right)^2+2\nu\left(\frac{\partial^2 Z}{\partial X^2}\right)\left(\frac{\partial^2 Z}{\partial Y^2}\right)+2(1-\nu)\left(\frac{\partial^2 Z}{\partial X\partial Y}\right)^2\right]\partial X\partial Y \tag{5.5}$$

where

$$D=\frac{Eh^3}{(12(1-\mu^2))} \quad \text{(plate stiffness factor)}$$

E = modulus of elasticity

h = plate thickness

ν = Poisson's ratio

$$T = \frac{\rho\Omega^2}{2}\int_0^a\int_0^b Z^2 dXdY \tag{5.6}$$

where ρ = mass per unit area

Ω= frequency, radians per second

Performing the derivatives and integrals required by the equations (above) produces the following:

$$V = \frac{\pi^4 DZ^2 ab}{8}\left(\frac{1}{a^4} + \frac{2}{a^2b^2} + \frac{1}{b^4}\right) \tag{5.7}$$

$$T = \frac{\rho\Omega^2}{2}\left(\frac{Z^2 ab}{4}\right) \tag{5.8}$$

Assuming no energy is lost, the strain energy of the vibrating plate must equal the kinetic energy. These two equations are then equated and solved for Ω^2 . The frequency of the circuit board with all four sides simply supported, in Hertz, is then

$$f_n = \frac{\pi}{2}\sqrt{\frac{D}{\rho}}\left(\frac{1}{a^2} + \frac{1}{b^2}\right) \tag{5.9}$$

This same procedure can be used for any boundary conditions to determine the fundamental frequency. The equation for two sides simply supported and two sides clamped, which is the other case analyzed here, is

$$f_n = \frac{\pi}{3.46}\left[\frac{D}{\rho}\left(\frac{16}{a^4} + \frac{8}{a^2b^2} + \frac{3}{b^4}\right)\right]^{1/2} \tag{5.10}$$

As can be seen from the equations, the natural frequency of the circuit boards is a function of size (a, b), stiffness (D), and mass per unit area (ρ). Increases in mass and/or board size will lower the natural frequency. Increases in thickness and/or modulus of elasticity will increase the frequency.

Spreadsheets using Lotus 1-2-3 were used to analyze the two EPS circuit boards for fundamental frequency. These spreadsheets are in Appendix D.

The mass per unit area includes the mass of the board plus the mass of the components. For the logic board this was 0.54 pounds and for the switch board it was 0.75 pounds.

Card-loks vary in effectiveness depending on the stiffness of the circuit board . They do not provide a completely clamped edge. With lower board natural frequencies, the card-lok is able to rigidly hold the edge so that no rotation occurs. As the frequency increases, it is not able to do so as well. Some rotation occurs. The "percent fixity" can be determined based on the frequency, and a more accurate value for the board frequency can be obtained.

$$f_n = f_s + P_f(f_f - f_s) \tag{5.11}$$

where

f_n = natural frequency

f_s = natural frequency with simply supported edges

f_f = natural frequency with clamped sides

P_f = percentage fixity

A value for percentage fixity cannot be determined until the resonant frequency is known, however the natural frequency, f_n , can be solved for directly without knowing percentage fixity using

$$f_n = \frac{f_s + 1.10(f_f - f_s)}{1 + 0.001(f_f - f_s)} \tag{5.12}$$

Table 3 gives the frequencies obtained for both circuit boards for the four sides simply supported, and two sides supported, two sides clamped boundary condition cases. Results using equation (5.12) are also listed.

	Weight (pounds)	f_s (Hz)	f_f (Hz)	f_n (Hz)
Logic Board	0.5	68.7	109.0	108.7
Switch Board	0.8	58.5	92.9	93.2

Table 3. Circuit Board Natural Frequency

2. Deflection

Values for deflection using both methods can now be obtained. The values obtained for frequency can be placed into equation (5.3) to obtain values for deflection. Tables 4 and 5 list the values calculated for each circuit board for deflection using both methods. Deflection is listed in units of 'mils', which are thousandths of an inch.

Board	Boundary Conditions	Deflection (mils)
Logic	Simply supported (method 1)	32.7
Logic	Sides clamped	94.7
Logic	Simply supported (method 2)	189.5

Table 4. Logic Board Classical Deflection

Board	Boundary Conditions	Deflection (mils)
Switch	Simply supported (method 1)	45.1
Switch	Sides clamped	120.3
Switch	Simply Supported (method 2)	240.9

Table 5. Switch Board Classical Deflection

The results of both methods vary significantly from each other. The discrepancies between the two methods are probably due to the different assumptions used to develop the formulas, which can be seen from the different parameters in each equation. In all cases the deflection is high. It is desirable that it be reduced below 10 mils.

3. Stiffener

One way to decrease the deflection is by adding a stiffener. This changes the plate stiffness factor, D. The plate stiffness factor used in the equations for both methods presented so far has been for an isotropic plate. A stiffener changes this, so that D has different values in the X and Y direction.

Stiffeners are typically made of steel, copper, brass, aluminum or fiberglass [Ref. 8]. These materials have high modulus of elasticity which increases the stiffness of the entire board. Space use limits the materials available, as do requirements for thermal control and circuit board wiring. Circuit boards with ribs made of metal must be designed carefully so that they do not cause electrical shorts by coming in contact with the board wiring. The satellite is being constructed predominantly of aluminum, as this material is easier to work with, so it was chosen as a stiffener material.

The effect of an orthotropic stiffness factor, D, was not considered for the first deflection method (Eqn 5.1). Its affect on natural frequency and deflection using equation (5.3) was considered.

The equations for natural frequency must be modified to include the directionality of the stiffness factor in the case of a stiffener. The simply supported equation becomes

$$f_n = \frac{\pi}{2}\left[\frac{1}{\rho}\left(\frac{Dx}{a^4} + \frac{4Dxy}{a^2b^2} + \frac{Dy}{b^4}\right)\right]^{1/2} \qquad (5.13)$$

where D_x is the bending stiffness along the X axis and D_y is the bending stiffness along the Y axis. D_{xy} is the torsional stiffness of the circuit board and stiffener.

The stiffener will be located at the center of the board, connecting the two sides which are held in place by the card-loks. This is along the X axis of the board. As a result, the stiffener will have no impact on the bending stiffness along the Y axis. D_y will remain the same as D in the case without a stiffener.

To calculate the bending stiffness in the X direction, D_x , the circuit board and stiffener are analyzed together. The cross sectional view appears in Figure 13. The circuit board is item #1 and the stiffener is item # 2.

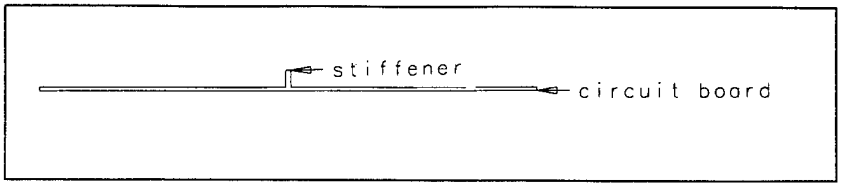


Figure 13. Circuit Board with Stiffener

The stiffener changes the moment of inertia of the circuit board. The X direction stiffness is given as

$$Dx = \frac{EI}{d} \tag{5.14}$$

where

$$EI = \Sigma EI_o + AEc^2 \tag{5.15}$$

E = modulus of elasticity

I_o = moment of inertia for one item

A = Item area

c = distance from item centroid to centroid of stiffener and rib

d = rib spacing, if more than one rib is used

Appendix E contains the spreadsheets used to calculate EI for the circuit board with the rib. The size of the rib and the material used to make it have a large impact on the value for EI and D_x. Several cases were analyzed using different size ribs to determine the effect on EI and consequently on the frequency and deflection.

The other term in the modified equation for natural frequency is D_{xy}, given by

$$Dxy = G_e J_e + \frac{G_r J_r}{2d} \tag{5.16}$$

where

G_e = shear modulus of circuit board

$J_e = h^3/3$ = unit torsional stiffness of circuit board

G_r = shear modulus of stiffener

J_r = torsional stiffness of rib

d = rib spacing

D_{xy}, torsional stiffness, is a function of the dimensions of the stiffener. Detailed calculations are also found in Appendix E. The same variations in rib sizing used in determining D_x were analyzed for D_{xy} also.

With values for D_x, D_y and D_{xy}, the natural frequency of the circuit board which is simply supported on all four edges and uses a stiffener can be calculated. The spread sheet in Appendix E shows the frequencies for each rib analyzed. The results are summarized here in Table 6.

Rib Size (mils)	D_x (N-m)	D_y(N-m)	D_{xy}(N-m)	f_s (Simp Sup) (Hz)	Deflection (mils)
300 x 125	126.3	5.4	11.6	180.8	44.3
400 x 125	261.7	5.4	12.3	244.4	28.2
300 x 200	184.4	5.4	18.0	219.3	33.2

Table 6. Direction dependent stiffness factors for switch board

The equation for two sides simply supported with two sides clamped also must be modified. An exact equation for this case was not found, but an approximation was made based on the form of the modified equation for four sides simply supported. This modified equation was

$$f_n = \frac{\pi}{3.46}\left[\frac{1}{\rho}\left(\frac{16Dx}{a^4} + \frac{16Dxy}{a^2b^2} + \frac{3Dy}{b^4}\right)\right]^{1/2} \qquad (5.17)$$

The frequencies obtained for natural frequency in both cases were combined as before to determine an improved natural frequency for the circuit board with stiffener. This improved natural frequency was used in the deflection equation to determine the deflection. The results for the three different rib possibilities are shown in Table 7.

Rib (mils)	f(ss) Hz	f(ss+clamp) Hz	f_n Hz	Deflection (mils)
300 x 125	180.8	378.1	332.3	17.8
400 x 125	244.4	534.6	436.8	11.8
300 x 200	219.3	457.5	388.7	14.1

Table 7. Switch Board with Stiffener

The stiffener clearly increases the frequency of the circuit board, reducing the deflection.

C. FINITE ELEMENT MODEL ANALYSIS

Both the logic and switch boards were modeled in I-DEAS using thin shell elements. Finite element model analysis in general will give better answers as the number of nodes and elements are increased. To determine how the number of nodes used in a model might affect the results obtained, two models were made for the logic board. Each model was solved for frequency using a dynamics solution and for stress using the linear statics solution. The results were compared to simple hand calculations. One model had 25 elements and the second had 1750 elements. Both cases used simply supported edges as boundary conditions and neither included the stiffener. The results are included in Table 8, along with the hand calculations.

	Freq (Hz)
25 elements	67.2
1750 elements	68.5
hand calc	68.7

Table 8. Comparison of Logic Board Finite Element Models

This may lead to a temptation to make a model with a large number of nodes and elements to improve accuracy. However, processing time increases significantly as the number of nodes is increased. The dynamic and static solutions for the 25 element model took one minute each. The solutions for the 1750 element model required 20 minutes each. Larger models require increasingly greater amounts of processing time. In the

preliminary design phase, "ball park" solutions are sought. Several different designs are usually being considered and answers that are correct to an order of magnitude are usually sufficient at this point. The user must consider if the additional accuracy merits the extra computational time. Once a final design has been selected, a very detailed finite element model is made and analyzed.

1. I-DEAS Models

Finite element models were made for the logic and switch board, with and without a stiffener. Two stiffeners were used, each 0.0938 inches wide. One was 0.3 inches in height and the second was 0.4 inches in height. Each model was analyzed with boundary conditions of all four sides simply supported and with two sides clamped and two sides simply supported. A linear static solution and a dynamic solution was done for each case. All models used thin shell elements for the circuit board and solid brick elements for the stiffener. The results are listed below in Tables 9 and 10 and graphed in Figure 14. Figures 15 and 16 show the logic board in its fundamental frequency mode with and without a stiffener. The 1750 element FEM is shown.

The values listed for stress in Table 9 are the highest stresses occuring in the model. For the circuit boards without a stiffener the highest stress was at the edges. For the circuit board with the stiffener the highest stress was in the stiffener, while stress in the circuit board was lower by a factor of two to three than in the stiffener . This is expected as the stiffener carries a significant portion of the load.

Board	Boundary Conditions	Natural (Hz) Frequency	Deflection (mils)	Stress(psi)
logic	SS	68.5	36.2	622.0
logic	CL + SS	106.5	15.1	532.0
logic (0.3 stiff)	SS	174.9	5.3	1,340.0
logic (0.3 stiff)	CL + SS	201.4	4.2	966.0
logic (0.4 stiff)	SS	198.1	4.3	820.0
logic (0.4 stiff)	CL + SS	219.0	3.7	658.0

Table 9. I-DEAS Results For Logic Board

Board	Boundary Conditions	Natural (Hz) Frequency	Deflection (mils)	Stress(psi)
switch	SS	58.4	50.0	857.0
switch	CL + SS	90.8	20.8	732.0
switch (0.3 stiff)	SS	149.4	7.3	1,810.0
switch (0.3 stiff)	CL + SS	172.1	5.7	1,300.0
switch (0.4 stiff)	SS	169.0	5.9	1,100.0
switch (0.4 stiff)	CL + SS	186.8	4.9	884.0

Table 10. I-DEAS Results for Switch Board

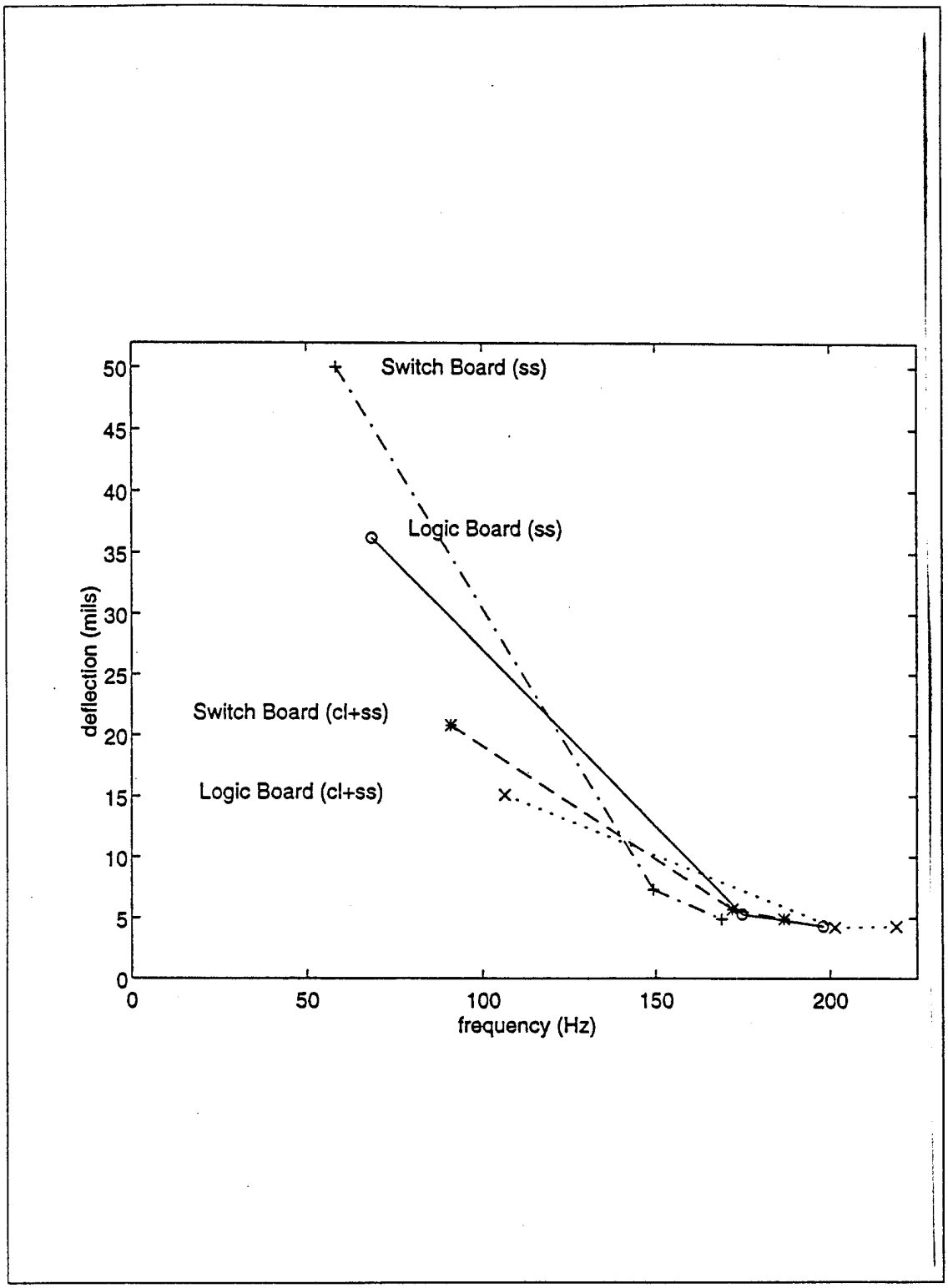


Figure 14. Deflection vs. Frequency For Circuit Boards

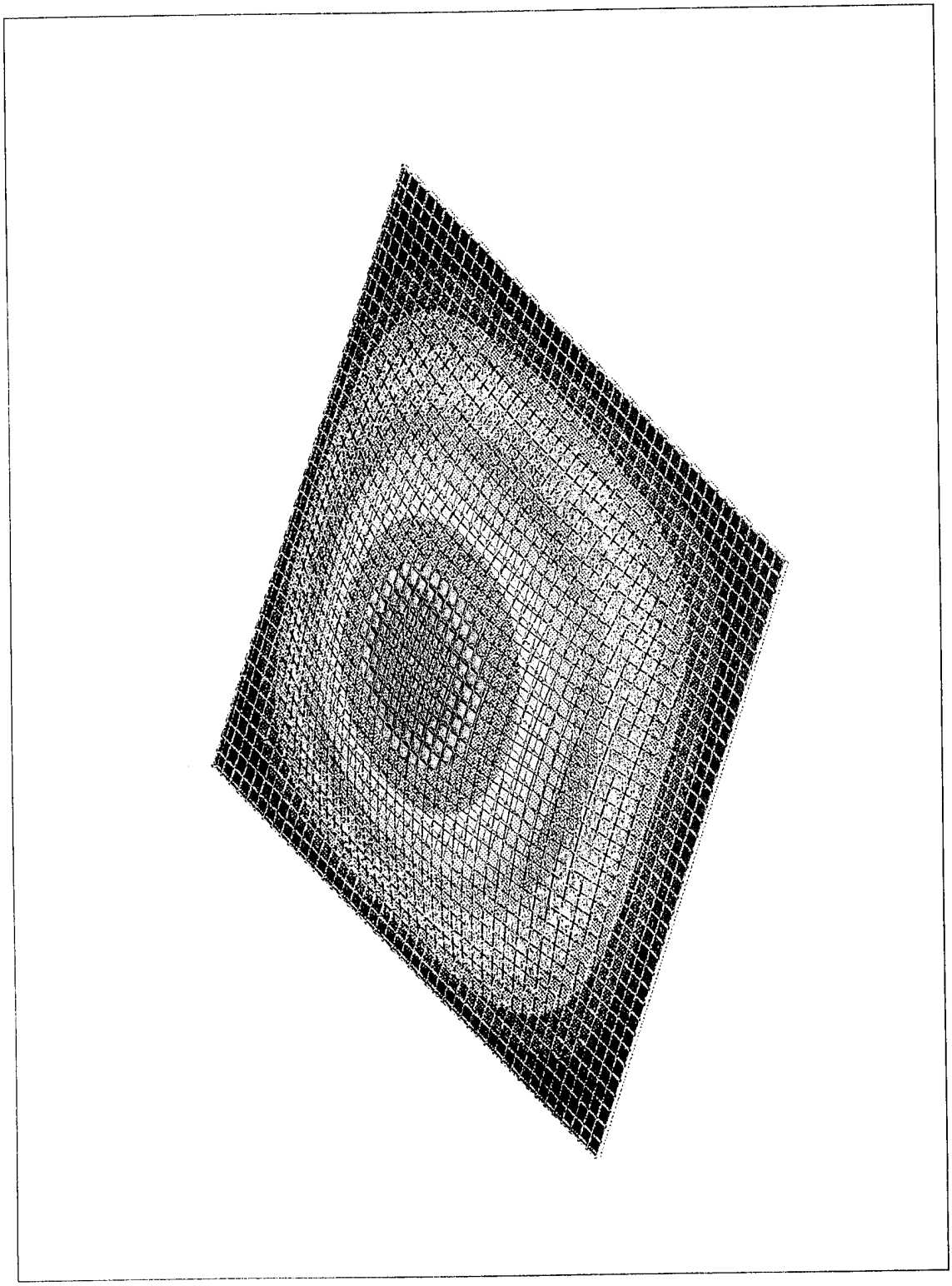


Figure 15. Logic Board Without Stiffener

D. DISCUSSION

The main purpose of the analysis was to determine the deflection of circuit boards. This was important in finding out if the stress levels in the component lead wires might be too high, which would lead to a failure.

Depending on the method used, however, there is a significant difference in the values obtained for deflection. In the simply supported case for the logic board without a stiffener, the method relating deflection to G forces and frequency gave a deflection 189 mils. The I-DEAS FEM gave a value of 36.2 mils. The frequency in each case was the same. Some assumptions were made in developing the equation, such as treating the circuit board as a single degree of freedom system. This may be one reason the values are not close, even though the frequencies are. The method relating deflection to load and stiffness gave values for deflection which were close to the I-DEAS FEM. The former gave 32.7 mils, the latter gave 36.2 mils. Similar discrepancies between the classical methods and the I-DEAS FEM exist in the other cases as well.

While there are differences in values between the different methods, the desired trends are present. In all cases higher frequencies did produce lower deflections. This can be seen more clearly in Figure 14, which graphs the I-DEAS results. Clamped boundary conditions had higher frequencies than simply supported boundary conditions. Frequencies for the switch board, which was heavier than the logic board, were lower than for the logic board in each case. These results were all expected, and these trends are obvious in all the results.

In all cases of the circuit boards without a stiffener, the deflection was larger than desirable, even though there were discrepancies between the various methods used. This indicates the need for a stiffener.

The frequencies obtained from the I-DEAS FEM and the classical method for the simply supported cases without a stiffener were very close. With the stiffener added, the frequencies began to diverge. This can be seen by comparing natural frequencies for the switch board with stiffeners in Tables 6 and 10 . The difference increased as the stiffener

size increased. However, the general trends are present as expected. The larger stiffeners did increase frequency and reduce deflection.

The differences point out some of the problems inherent in attempting to develop accurate models. The real proof of this analysis will come from actual testing. The fact that different deflections are produced also highlights the need for testing to verify the actual effects of the launch environment.

VI. EPS HOUSING

A. FINITE ELEMENT MODEL

The EPS housing was analyzed using I-DEAS to determine its natural frequency and the stress levels it would experience during launch to ensure these values were within the design criteria. I-DEAS was used to make a simple model of the housing for analysis, using the loads set forth in Chapter I for non structural components. The model was a hollow box with dimensions of 2 x 8.5 x 10 inches with walls 1/16 inch thick. The simplified model provided rough estimates of stress and natural frequency which were compared to the design criteria. It served as a limiting case since the housing was actually thicker in several places and therefore the real natural frequency would be higher.

Two finite element models were made to determine an appropriate element size. Two I-DEAS solutions were run on each model: linear static and normal mode dynamics. Both models were made with thin shell elements using a mapped mesh. The first model used elements that were 0.2 inches in size. It had 5738 elements and 5740 nodes. The second model used 0.5 inch elements and had 928 elements and 930 nodes. The first model required 20-30 minutes to solve for linear statics and normal mode dynamics. The second model solved both cases in approximately two minutes. Figure 17 shows the second model in its first mode of vibration.

Table 11 lists the values obtained for natural frequency and stress. There is a 0.44% difference in frequency between the two models. There is a 25.9% difference in stress values. These results show that element size can be a critical factor, depending on the type of solution desired. For frequency the error is insignificant, for stress it is not.

Model	Natural frequency (Hz)	Stress (psi)
one	227.0	704.0
two	228.0	518.0

Table 11 EPS Test Finite Element Model Results

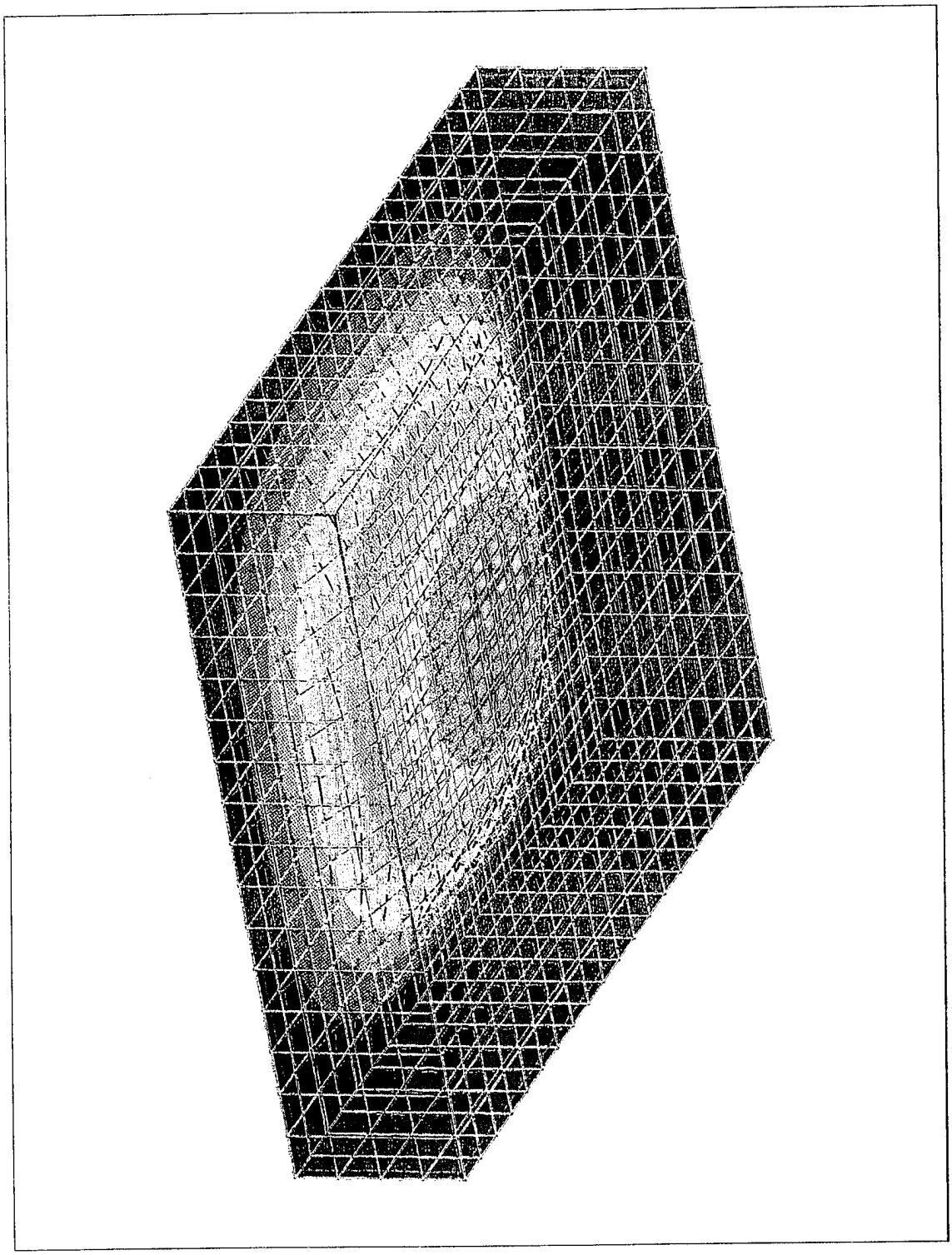


Figure 17. EPS FEM in Fundamental Frequency Mode

The stress obtained, 704 psi, for the first model, is still considerably less than yield stress for 6061 aluminum (36,000 psi). Inserting these values into equation 1.1, and assuming a large safety factor, the margin of safety is well over 0, as required. The natural frequency is well above the minimum required by the GAS CAN program, and is different from the circuit boards as well. This is important because it is desirable that the resonant frequencies of the housing and the circuit boards not be coupled. These parameters are well within their design criteria.

B. MANUFACTURING

1. Machining Limitations

The actual construction of the housing was dictated by the equipment available at NPS. Ideally the housing should be made of as few pieces as possible. This helps reduce problems when the parts are fitted together. It is also stronger structurally and more effective in EMI shielding.

Limitations imposed by the machining equipment led to four pieces being used for the housing. These are shown in the exploded view in Figure 9 and in Figures 18-21 in this section. The biggest piece is the sides and bottom, which were made from one piece of aluminum. The sides have gaps cut out for the card-loks. There are also flanges at the top along both sides which are used for the screws which join the housing with the upper equipment plate.

The gaps for the card-loks are 0.3125 inches high and 0.25 inches wide. These measurements are determined by the Series 230 card-lok selected for the circuit boards. The gaps extend nine inches from the front of the housing toward the rear. In the last one inch the 0.25 inch ledge between the gaps has been removed. This space has been reserved for the motherboard.

The top cover is made from a separate piece of aluminum. Ideally it would be made from the same piece as the sides and bottom. However, the cutting tool cannot

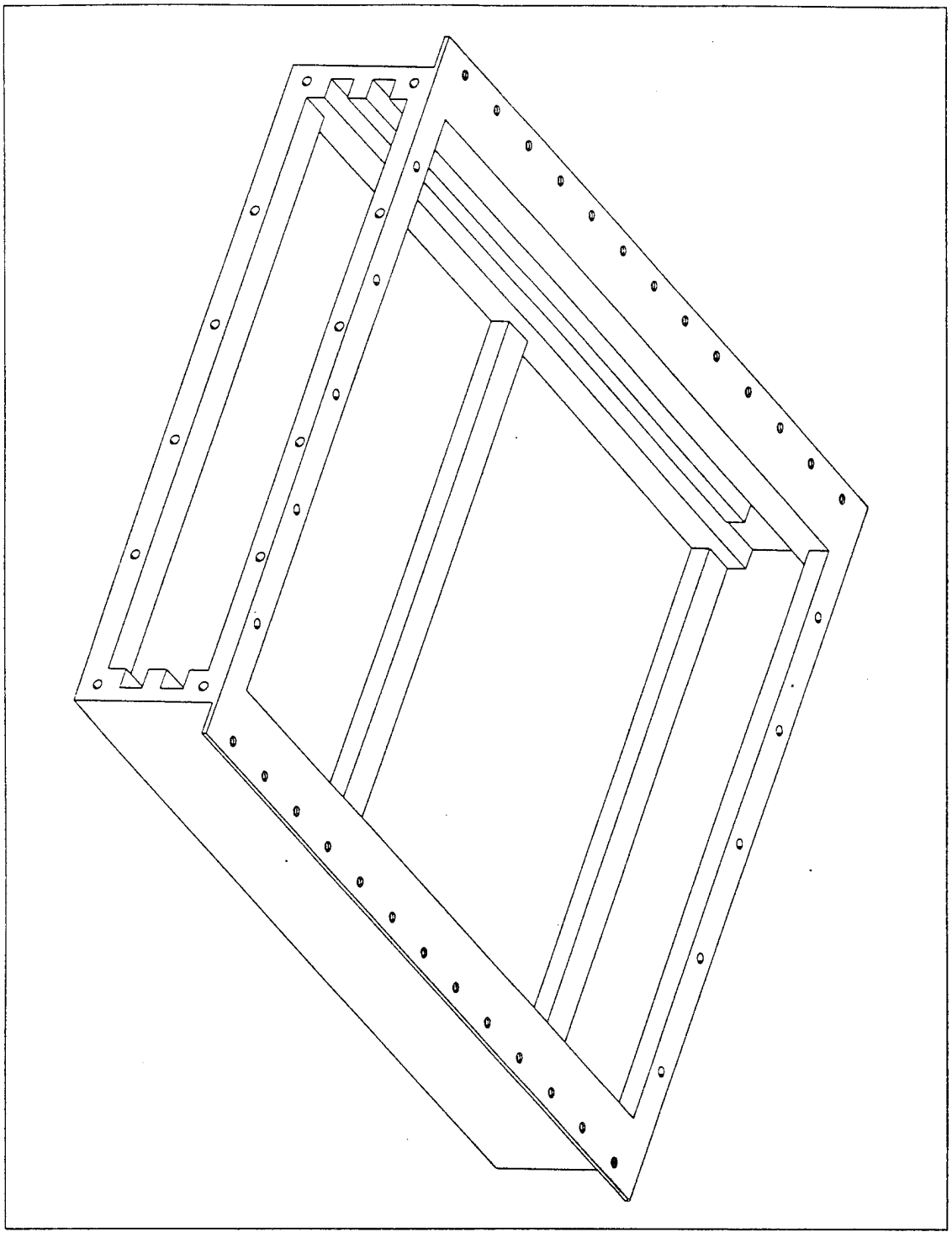


Figure 18. EPS Housing Main Body

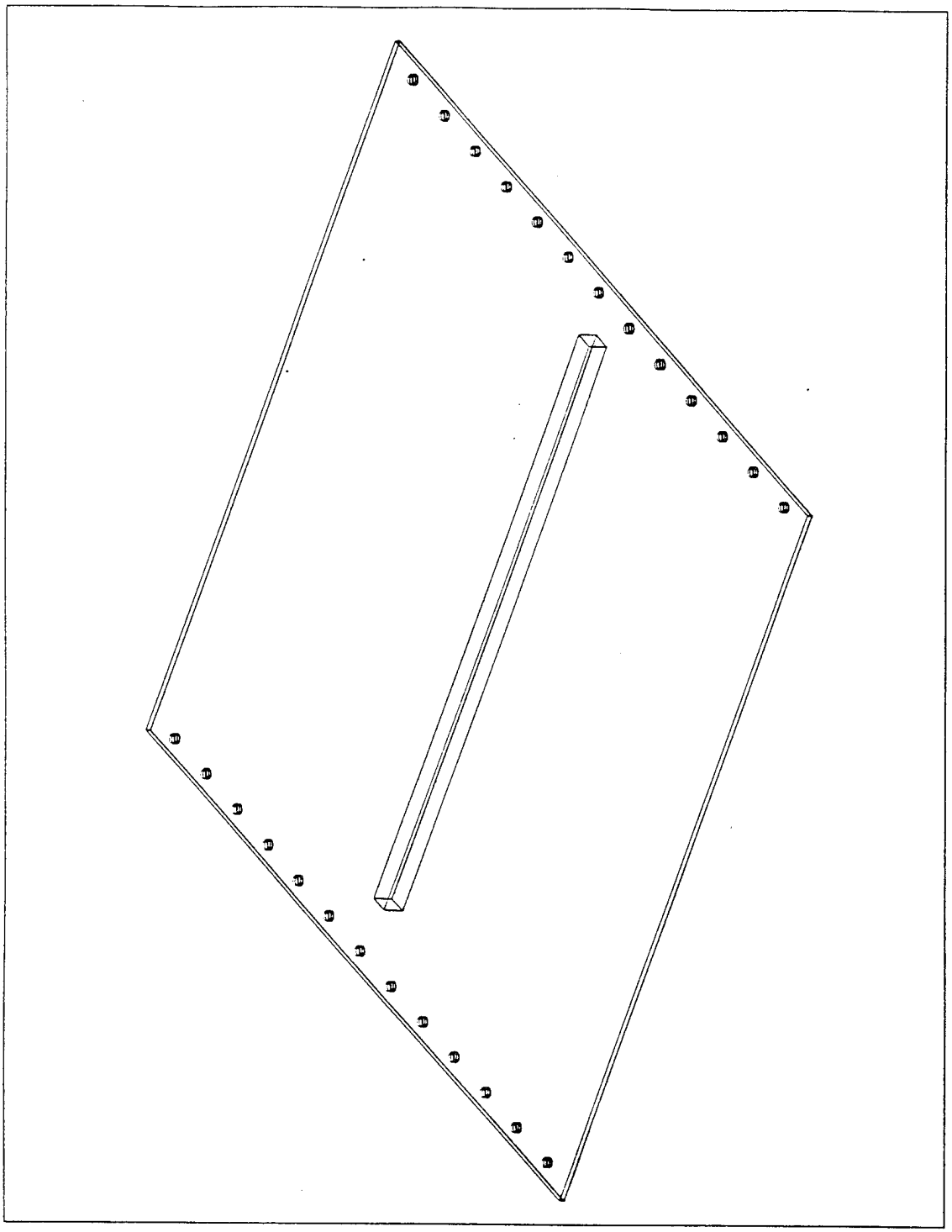


Figure 19. EPS Housing Top Cover

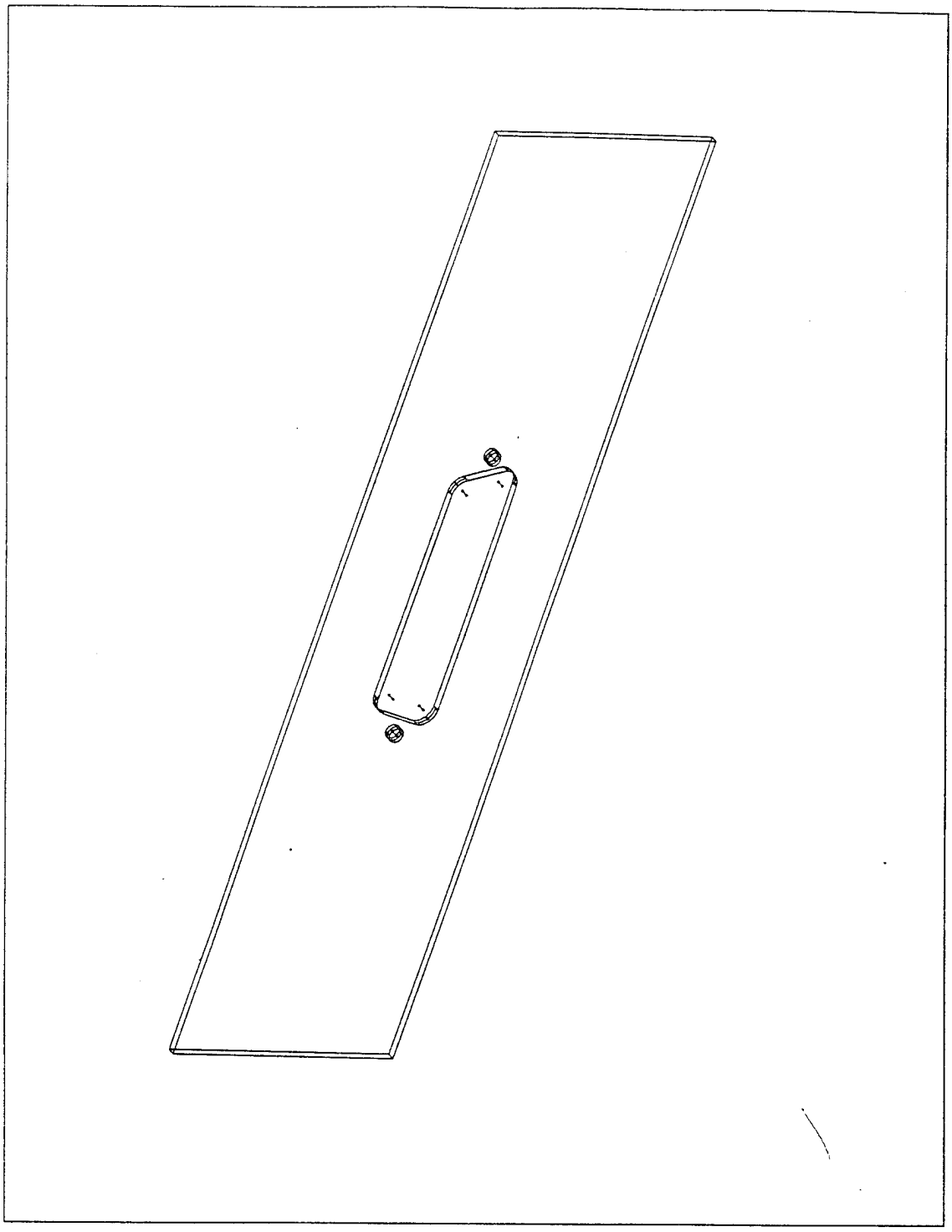


Figure 20. EPS Back Cover

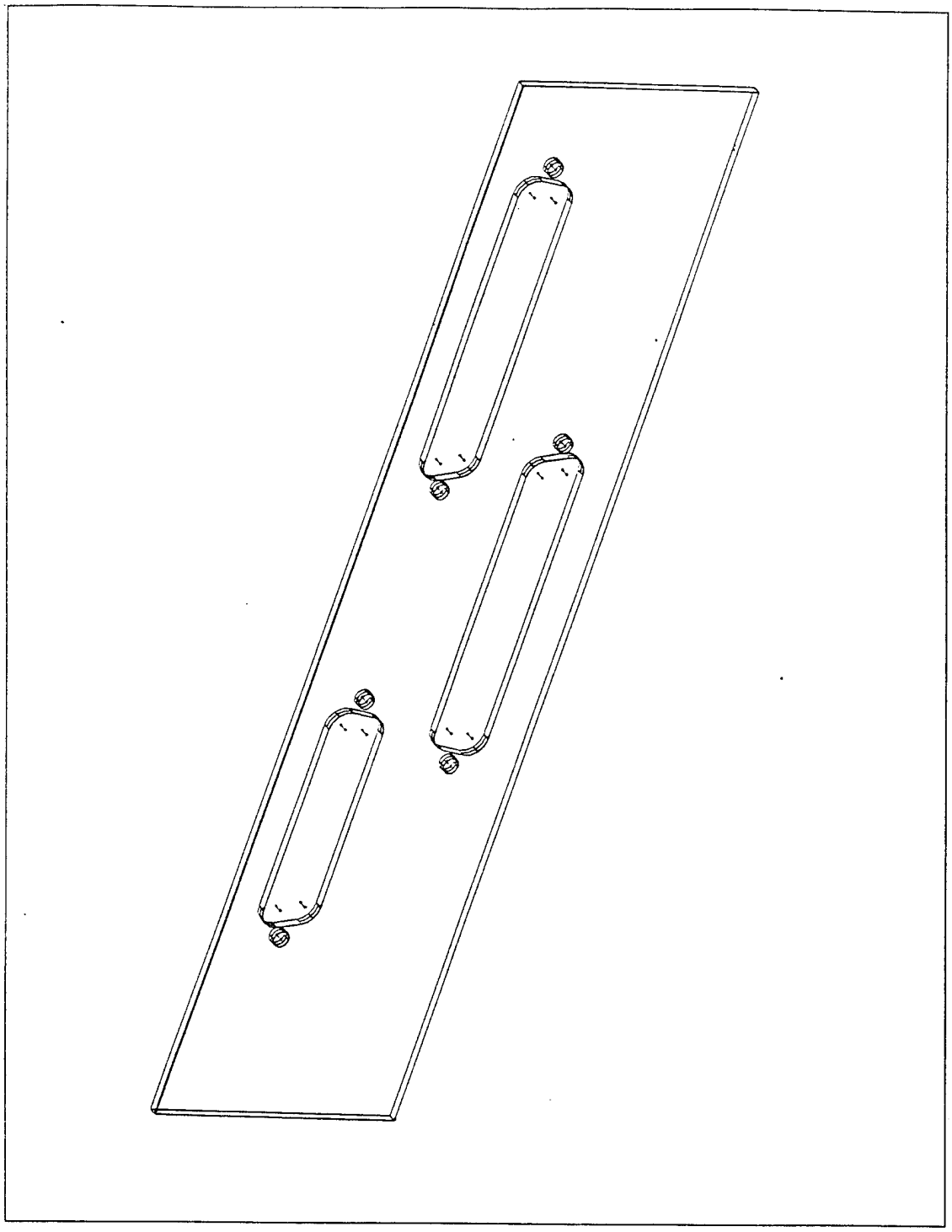


Figure 21. EPS Front Cover

maintain the required tolerances to cut out the card-lok gaps by proceeding from the front, to the back 10 inches away.

Two stiffeners have been built into the top cover and bottom surface of the main body of the housing. This material has been left to stiffen the housing and increase its natural frequency.

The front and back covers may need to be removed to provide access to the logic and switch boards and the mother board. They are made from separate pieces of aluminum to allow for this and have cut outs for the D-connectors.

Detailed dimensions of each piece can be found in Appendix F. The cutout sizes for the D-connectors are listed in Appendix A.

2. Joining

The separate pieces of the housing must be joined together, and the housing as a whole must be attached to the upper equipment plate. Screws are used for this purpose. Welding was considered for joining the top cover to the sides but this ideas was discarded because the heat produced would warp the cover.

Second only to the circuit board size, the type and location of the screws had the largest impact on the dimensions of the housing. The walls had to be made thicker than structurally required in order to provide space for the screws to be inserted, with enough room on either side of the screws to maintain structural integrity.

Number 4 socket head screws are used in the housing. These screws have a 0.112 inch shaft diameter with 40 threads per inch. Socket heads were selected because they are easier to work with when loosened or tightened. Figure 22 shows a socket head screw.

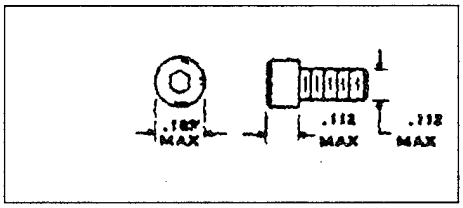


Figure 22 . Socket Head Screw

When positioning screws caution must be used to ensure the screw does not protrude through the housing walls into the interior of the housing. Aluminum material might otherwise be inadvertently pushed into the housing when the screws are inserted. This material might damage the circuit boards, possibly causing electrical shorts. The flange on the sides of the housing has been added so that screws used to attach the top cover to the housing and the housing to the equipment plate will not go inside the housing. Where there is not enough space to add a flange, blind tap holes are used. These holed do not go completely through the walls. A small pocket at the bottom of the hole contains any material loosened by the screw as it is inserted. Figure 23 shows a blind tap hole.

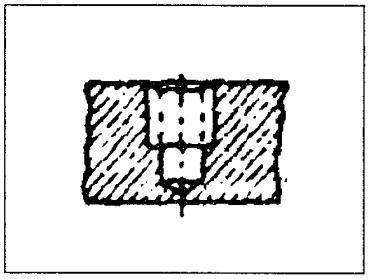


Figure 23 . Blind Tap Hole

The housing will be joined to the upper equipment plate before the front and back covers are attached. The screws will come through the equipment plate, top cover and the flanges on the housing sides. The same screws are used to attach the top cover to the housing and the housing to the equipment plate. This reduces the number of screws and holes needed and also simplifies the design of the top cover slightly.

Socket head screws with washers and nuts are used along the sides of the housing. The screw is counter bored into the equipment plate. The head does not protrude from the equipment plate which prevents any potential interference with components on the upper surface of the plate. Tap holes are drilled through the top cover and the flange on the side of the housing. The total distance through the three pieces is 0.375 inches. Accordingly a half inch screw is selected. Flat washers are placed at both ends of the

screw, and a nut is attached to the screw as well. This arrangement is shown in Figure 24, without nuts and washers.

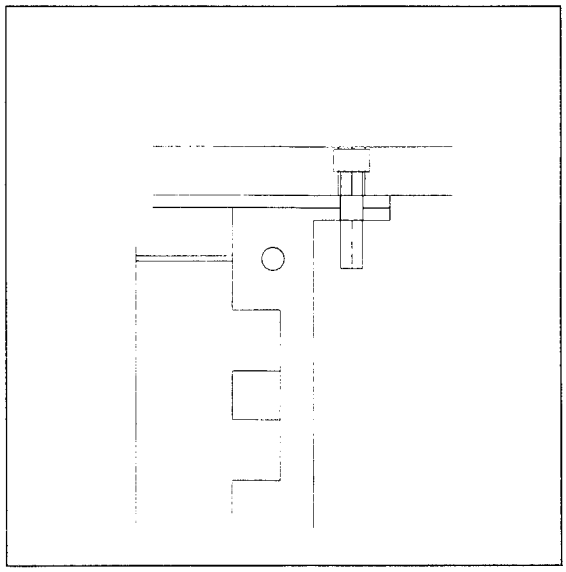


Figure 24. Housing Attachment to Equipment Plate

Blind tap holes are used to attach the top cover and housing to the equipment plate at the front and back. The screw cannot go through the housing or it would protrude into its interior. A flange similar to the one on the side of the housing is not practical because screws extending all the way through would interfere with the face cover as it is attached or removed.

Blind tap holes are also used to attach the front and back covers to the housing. Again the screws may not protrude into the housing, and flanges are not practical which leads to the use of blind tap holes.

The locations of the screw holes from the edges of the housing is also important. Their approximate locations are shown in Figure 25. As a rule of thumb the distance from the centerline of the screw to the edge should be one and a half to two and a half times the screw diameter. For the 0.112 inch diameter screw used in the housing this equates to 0.168 to 0.280 inches. The housing is designed to accommodate this. On the top, the edges are 0.825 inches wide, including the flanges. The front and back edges are

0.425 inches wide. The front and back faces of the housing have edges which are 0.338 inches at the bottom and 0.275 inches at the top. The bottom edge is just large enough for the screw to fit with one and a half times the diameter on either side. The top edge is too small, and cannot be made larger due to minimum circuit board clearance requirements. Since the top cover will be added and the equipment plate is above that, the screw is positioned so that 0.168 inches is available below it. The presence of the top cover and equipment plate should counter any potential problem caused by the short distance from the screw to the edge.

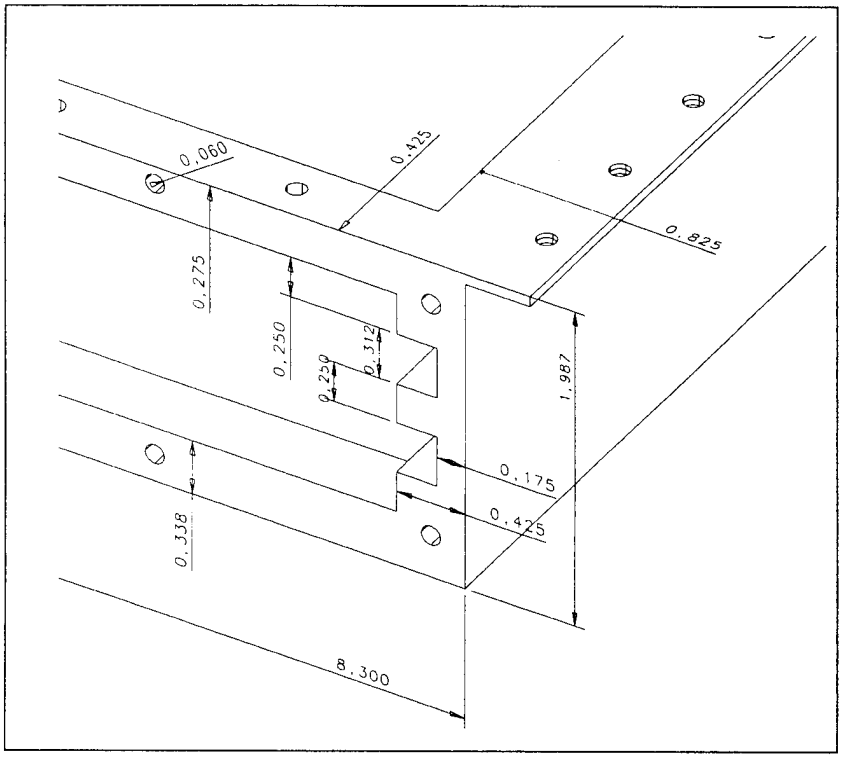


Figure 25. Fig w/ dimensions

Distance between the screws is mostly a function of allowable pressure differential, which relates to EMI. This is discussed in detail in the following section. Where practical screws are space every 3/4 inches. Since screws are going into the housing front and back faces from the top cover and front and back covers, these screws are spaced approximately one and a half inches apart (1.49 inches).

C. ELECTROMAGNETIC INTERFERENCE (EMI)

Electromagnetic Interference (EMI), also called noise, is an issue which can be of great concern in electronic systems. Circuits operating in close proximity to each other may affect each other negatively, perhaps to the point where the system containing the circuits does not work. The exact manner in which circuits interfere with each other, or even if they will interfere with each other is difficult to predict. Actual testing with all systems in full operation is needed.

While it is difficult to know if circuits will interfere with each other, there are several items which can be considered during design which will minimize any potential EMI issues. The designer may consider these items and incorporate them during the process, or he may ignore them as he works and then analyze the finished product for noise effects. The first method is referred to as the "systems approach". The second method is called the "crisis approach". Examining EMI with the "systems approach" is recommended. It is usually much easier and less expensive to correct potential problems at this point than to put a "Band-Aid" on problems discovered after the design is complete.

The EPS logic and switch boards do not appear to be EMI sensitive components, or significant noise sources. This will not be verified until testing. Because of this, a systems approach is used here to include EMI reduction features in the design to minimize any potential problems. Actual testing will be needed to confirm no EMI problems exist.

1. EMI Sources

EMI can create problems in an electronic system three primary ways. A circuit can be affected by its own electromagnetic (EM) waves. This is called internal noise generation. A circuit can be affected by EM radiation from other nearby circuits, and a circuit can generate EM radiation which affects other circuits. In addition to radiation,

noise can also be transmitted by conduction. Lines passing through noisy environments can pick up the noise and conduct it throughout the system [Ref. 11].

Digital and analog systems are affected differently by the three sources mentioned. Analog circuitry is more susceptible to externally generated noise. Digital circuits operate at relatively large signal levels compared to analog circuits and are not as susceptible to external EM waves. Digital circuits are affected more by internal noise sources.

2. Internal Noise

As an example of how internal noise can affect a circuit, consider the following digital example. Information is passed in the form of 1's and 0's. A 5 Volt signal represents a 1, and a 0 V signal is a 0. Realistically these voltages are not exact. A threshold is defined, above which the signal is considered a 1 and below which it is a 0. current flow will produce a voltage given by equation (6.1).

$$V=L\frac{di}{dt} \tag{6.1}$$

While the current flows may be low, their rapid switching rate can create a high voltage. If the speed is high enough the noise voltage produced may increase the voltage enough to turn a 0 into a 1.

Internal noise comes mostly from ground bus noise and power bus noise. Ground noise is the more severe problem. It is produced by transient power supply currents and signal return currents. The power supply transients can be controlled, while signal return currents cannot. Transient ground currents are a source of intra-system noise as well as conducted and radiated emissions.

To minimize internal noise, the ground impedance must be minimized. The impedance is in direct proportion to the length of the wires on the circuit board. Keeping these as short as possible is the first step to reducing EMI. There is a limit, however, as to how short the paths can be made [Ref. 11].

A second way to reduce the current inductance is by creating alternative paths for current flow, which are electrically parallel. The more paths there are, the lower the circuit inductance will be. The best possible case will be with a ground plane in the circuit board. This amounts to an infinite number of parallel paths. The disadvantage is that it requires a multilayered board which is more expensive. The EPS logic and switch boards are multilayered, however, and do include a ground plane.

Power supply transients are not as critical since they can be controlled. The use of a power plane will additionally reduce inductance. This requires a more expensive multilayered board, and again the EPS boards also include a power plane.

3. Radiation

Radiation generated by digital circuits is either differential mode or common mode radiation. Differential mode radiation is caused by current flowing in loops around the circuitry. The loops act like small antennas. Common mode radiation is due to undesired voltage drops in the circuit which cause some components to be at an equal potential which is higher than ground. External cables connected to the system can be affected by that common mode potential and also act like antennas.

Radiated emission can be minimized by carefully designing the board layout to keep the loop areas formed by the circuits as small as possible. The most critical loops are the ones involving the system clock because of its high frequency, periodic signal. Circuit board layout is beyond the scope of this report. In addition to layout, a ground plane is also very effective in minimizing radiated emission. A ground plane will reduce the voltage drop and minimize loop areas.

4. PANSAT Boards

Both the logic and switch boards are multilayered and have ground and power planes. Most of the circuitry is analog and only a small portion is digital. This will significantly reduce the noise effects they experience and cause. Many of the noise problems increase with speed. The logic used by the digital portion is CMOS, which is

fairly slow. Digital circuitry is most susceptible at speeds above 10 MHz, and PANSAT operates at less than 1 MHz.

The major noise producing item in the EPS system is the Simple Switcher Step Down Voltage Regulator used by the logic board to reduce spacecraft bus voltage from 15 volts to 5 volts for use by the system's digital circuitry. This switcher operates at 52 kHz. This frequency is well below the levels that typically cause EMI.

Another device used by the EPS system to minimize noise is a ferrite bead. These beads are used to prevent noise generated by the digital circuitry from getting to the analog circuitry via conduction. Ferrite is a generic term for a class of non-conductive materials. The ferrite beads are particularly effective in damping out high frequency oscillations generated by switching transients.

Because the EPS system is mostly analog, uses CMOS logic in its digital circuitry, has multilayered boards with a ground plane and power plane, and uses ferrite beads, noise is not expected to be a problem.

5. Testing

Due to the difficulty in actually predicting how or if EMI will be an issue, actual testing is needed. Differential voltage should be measured in several places around the boards. While slower CMOS logic can handle higher levels of noise, it is best to keep the noise differentials under 1 Volt. A ground plane can reduce the differentials to 150 - 300 mV or less. The PANSAT boards should be tested to ensure they meet the necessary performance requirements.

D. EMI SHIELDING

To reduce EMI, shielding may be used. A shield is defined as a metallic partition placed between two regions of space [Ref. 11]. It contains EM fields by surrounding the noise source. This helps provide protection for EMI susceptible equipment outside the source. It also helps keep radiation generated by other subsystems out. Shielding will minimize radiation effects, but precautions also must be taken with cabling passing

through the shield. Cabling can easily conduct noise into or out of a system, which can make the shield virtually useless. The effect of a shield is a function of the material used and the presence of any holes or discontinuities. The PANSAT EPS boards are supported in a housing. This housing meets primarily structural needs and also serves as a shield.

1. Shielding Material

As the EM wave propagates, it will contact the shield and some of the wave will be reflected and some will be transmitted. The amounts will depend on the material used. The energy transmitted will also be attenuated which is referred to as absorption loss. Absorption loss will increase as shield thickness increases.

A key item is the skin depth of the EM wave. Skin depth is the distance the wave will travel until it has been attenuated to a point where it is 37% of its original value. If the shield wall is at least as thick as the skin depth, a significant amount of the EM wave will be absorbed. Skin depth is a function of frequency and material. Table 1 shows values for skin depth at various frequencies for aluminum.

All of the EPS housing walls are at least 0.0625 inches thick. Most are thicker than this; for example the sides are 0.175 inches thick. From Table 12 it can be seen that the housing absorbs a considerable amount of EM energy except at the lowest frequencies.

Frequency (Hz)	Skin Depth (mils)
1,000.0	3.0
100.0	11.0
10.0	33.0
1.0	105.0

Table 12. Frequency and Skin Depth

2. EM Field Region

The EM field is broken into two regions: the near field and the far field. The near field is close to the source, within a distance equal to $\frac{\lambda}{2\pi}$ [Ref. 11]. Considering the

low frequencies generated by PANSAT and the satellite size, all PANSAT subsystems are in the near field. In this region the characteristics of the EM wave depend on whether the Electric Field or Magnetic Field dominates. This will depend on the voltages and currents involved and is beyond the scope of this report. It should be examined, however, since shielding is less effective against predominantly magnetic fields at low frequencies.

3. Apertures and Discontinuities

The ideal shield is a continuous, conductive enclosure with no openings [Ref. 11]. The EPS housing is not an ideal shield because manufacturing limitations have dictated that it be made of four pieces. Seams are formed where these pieces are joined together and cut outs have been made in the front and back covers. These joints and cutouts reduce the shielding effectiveness by allowing EM wave leakage.

The EM waves generated by the circuitry inside the shield sets up current flows in the shield walls when they strike the walls. These currents generate additional fields which cancel some of the original field. This is one of the ways shielding reduces EMI. The current flows are disrupted by seams and apertures. The disruption is significant enough that discontinuities have a much greater impact on the shield effectiveness than the material used does and steps need to be taken to reduce their impact.

4. Shielding Enhancements

EMI shielding degradation caused by seams and cutouts can be minimized several ways. The goal of each method is to provide electrical continuity across the joint.

One method is to ensure there is firm electrical contact at several points along a seam. The material on both sides of the seam should be conductive. A conductive coating can help. For the housing the aluminum walls are coated with alodyne.

Conductive gaskets can be used to provide electrical contact. Gaskets are placed in a groove on one of the pieces being joined. When the pieces are put together the gasket is compressed slightly and a good electrical contact is formed.

When gaskets are used along a seam joined by screws, the gasket should be placed between the screw and the inside of the housing, as shown in Figure 26. This protects against leakage due to the screw hole.

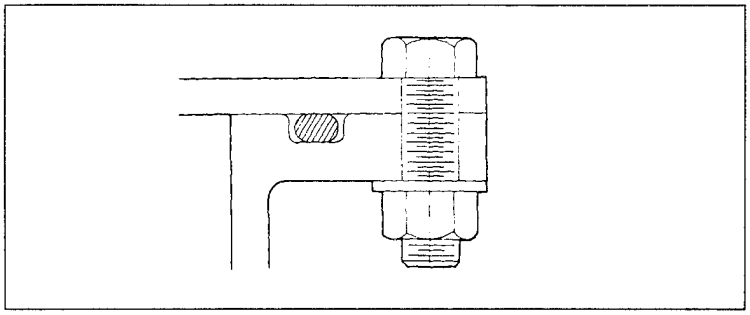


Figure 26. EMI Gasket Groove Placement [Ref. 10]

A disadvantage to using a gasket is that there must be a minimum area in which to place the groove. The space increases if screws are used. As shown in Figure 26, there should be area equal to the groove width on either side of the groove. Additional space must be available for the screw. For the screws and gaskets used in PANSAT, this minimum area is approximately 0.4 inches.

For areas that are not large enough, conductive sheet stock can be used. This material is cut to the desired size and shape and placed between the two pieces being joined. Screws used to join the pieces are placed through the sheet stock.

Other types of materials to reduce EMI leakage are available. The interested reader is referred to Reference 10, the EMI shielding handbook.

5. Shielding Enhancements for the EPS

Gaskets are used with the top cover of the EPS Housing and sheet stock is used for the front and back covers. The exact gasket to be used has not been selected, therefore the design does not show the groove. The width of the edges including the flanges is 0.825 inches, along the sides. The front and back edges, at the top of the housing, are 0.425 inches wide. This size was specifically chosen to allow a groove. The top cover is then placed onto the housing, compressing the gasket. Sheet stock is used between the

front and back covers and the housing. The edges here are not wide enough to allow a groove.

The distance between screws was determined by the allowable pressure differential for the effective use of the EMI gasket. The pressure between the surfaces joined will vary from a maximum at the screw location to a minimum half way between the screws. Pressure differential refers to the difference between the minimum and maximum pressures. The differential will decrease as the screws are placed closer together and increase as they are spread apart. To ensure a proper gasket seal the differential should be less than or equal to 10%. The pressure differential is a function of several factors in addition to screw spacing. These include flange width and thickness, modulus of elasticity of aluminum and foundation modulus of the seal. Detailed analysis has already been done, and guidelines are available for use in selecting screw spacing. For the housing the recommended spacing is 0.75 inches [Ref. 10].

To ensure these features adequately minimize any EMI problems, testing is recommended.

VII. CONCLUSION

I-DEAS software was used to develop a design for the PANSAT EPS housing and circuit boards. The software was also used to generate finite element models and analyze them for structural integrity. The results indicated that the designs easily met the requirements set forth by the Hitchhiker program for stress and natural frequency.

The results from I-DEAS varied significantly with other methods used to determine stress and natural frequency. These alternate methods, discussed in Chapter V, also indicated that the designs met the necessary criteria. The differences in results from the different types of methods used in the analysis could be due to several factors, including the assumptions used to develop each method. The boundary conditions and launch environment may have also been modeled with some inaccuracies.

The design has been developed only on software. In light of the variations in the analysis methods, and to ensure the design does meet the requirements, actual testing is strongly recommended. Valuable insights will be gained by building the housing and circuit boards. Inefficiencies introduced in the ways the parts are built and assembled are difficult to model. Testing will help ensure the design integrity.

The layouts of the logic and switch boards shown in Chapter II are current as of 1 May 1995. Minor modifications were still being considered and the actual layout may be different. Changing the layout may affect the weight of the board. The analysis done here was based on weights of the boards as of 1 May. A change in weight will change the results, although the general trends will still be the same.

The dimensions given through out the thesis are what is desired. Some error will be introduced when the housing is actually constructed. Machining tolerances are +/- 0.005 inches. Because of the tolerances, some components may not join exactly as planned. The problem is also a factor with the D-connectors in the housing. It may not be possible to ensure the wires from the back of the motherboard to the straight-in

connector will fit as planned. Because of this the wires are a little longer than they need to be. This will ensure tolerances are not a major problem with the connections.

It has been shown that the logic and switch boards will require stiffeners. The analysis was done assuming the stiffeners were made of aluminum. There is no requirement for this, and other materials are available. Additionally, the effectiveness of the stiffener will depend on how it is attached to the boards. Further analysis should be performed to determine what material is best and which mounting method is best. Similarly, the card-loks must be examined to see how they can be mounted to the circuit boards.

EMI was discussed in detail in Chapter VI. As mentioned, only actual testing will ensure EMI problems do not exist. The design includes space for EMI gaskets. Gaskets come in several different sizes and shapes, each of which require different groove sizes. Which particular gasket that will be used, or even if a gasket will be required, is not known. Therefore while space has been provided, a groove has not been added to the design.

A very robust design has been developed for the EPS housing and circuit boards. The analysis shows that the design will exceed the requirements mandated by the Hitchhiker program. To ensure these requirements are met, the next logical step is to proceed with testing.

APPENDIX A. CARD-LOKS AND D-CONNECTORS

A. CARD-LOKS

The card-loks are made by Calmark Corp. of San Gabriel, CA. The Series 230 model card-lok is used with the EPS and shown in Figure 27. More details are available in the Calmark Corp. catalog [Ref. 10].

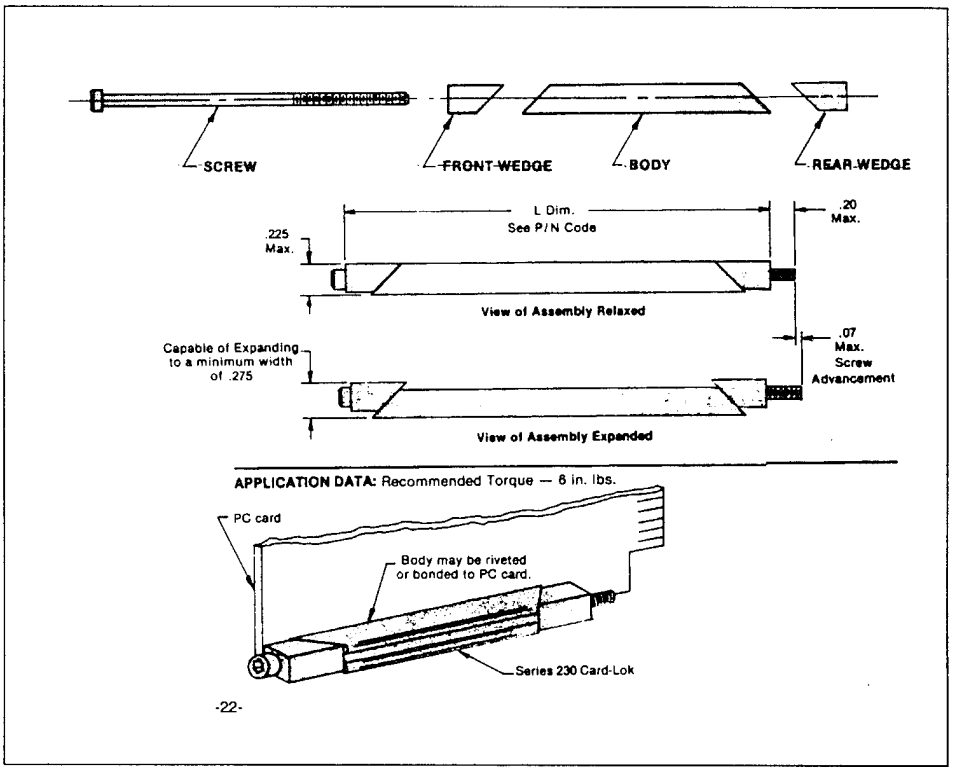


Figure 27. Card-lok [Ref. 12]

B. D-CONNECTORS

The D-connectors used are manufactured by Positronic Industries, Inc. of Springfield, Missouri. Four male D-connectors are used with the EPS housing and circuit boards. They are labeled J-21, J-22, J-23 and J-24 on the circuit board figures in Chapter II. J-21 is a straight mount connector, with 78 pins. The others are 90° mount connectors. J-22 has 62 pins, J-23 has 37 pins and J-24 has 25 pins.

Figure 28 and Table 13 give detailed dimensions of the connector shell assemblies. Measurements are in inches. Due to manufacturing similarities the 25 pin connector has the same dimensions as the 44 pin connector shown in Table 13. The 37 pin and 62 pin connectors also have the same size shell assemblies.

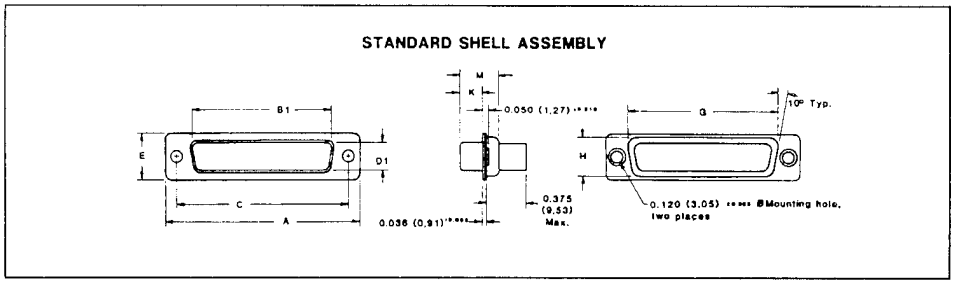


Figure 28. D-connector Shell [Ref. 13]

Conn.	A	B1	C	D1	E	G	H	K	M
J24	2.088	1.534	1.852	0.329	0.494	1.625	1.422	0.230	0.426
J23,22	2.729	2.182	2.500	0.329	0.494	2.272	0.422	0.230	0.426
J21	2.635	2.079	2.406	0.441	0.605	2.178	0.534	0.230	0.426

Table 13. Shell Dimensions

Cutouts were made in the front and back covers of the EPS housing for the D-connectors. Figure 29 and Table 14 show the details of the cutouts. Measurements are in inches. All connectors use rear panel mounts without a floating bushing.

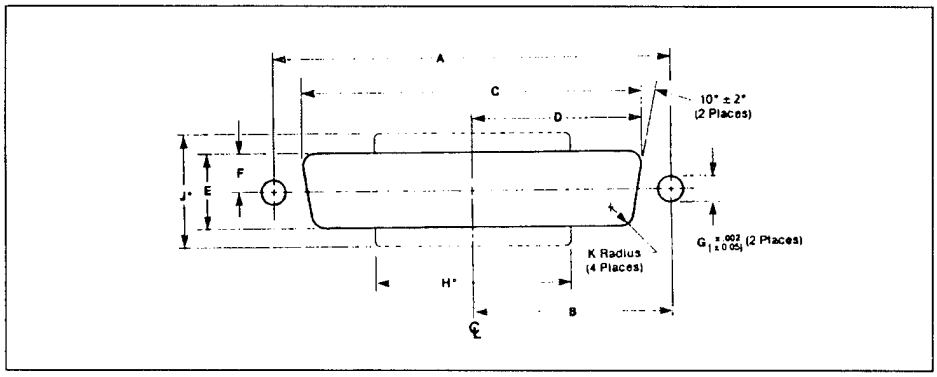


Figure 29. Shell Cutout [Ref. 13]

Conn.	A	B	C	D	E	F	G	H	J	K
J21	2.406	1.203	2.218	1.109	0.555	0.278	0.120	1.708	0.740	0.132
J22,23	2.500	1.250	2.326	1.163	0.449	0.225	0.120	1.813	0.630	0.132
J24	1.852	0.926	1.706	0.853	0.481	0.241	0.088	1.197	0.662	0.132

Table 14. Cutout Dimensions

APPENDIX B. EXPERIMENTAL DETERMINATION OF POLYIMIDE PROPERTIES

To determine the material properties of the circuit board, a loading test was done to two samples of the polyimide. These two samples were cut into the shape of a dog bone with a width of 2.75 inches and a height of 7 inches. See Figure 30. The test section was the middle portion of each sample. The larger top and bottom portions were used as grip areas for the testing machine.

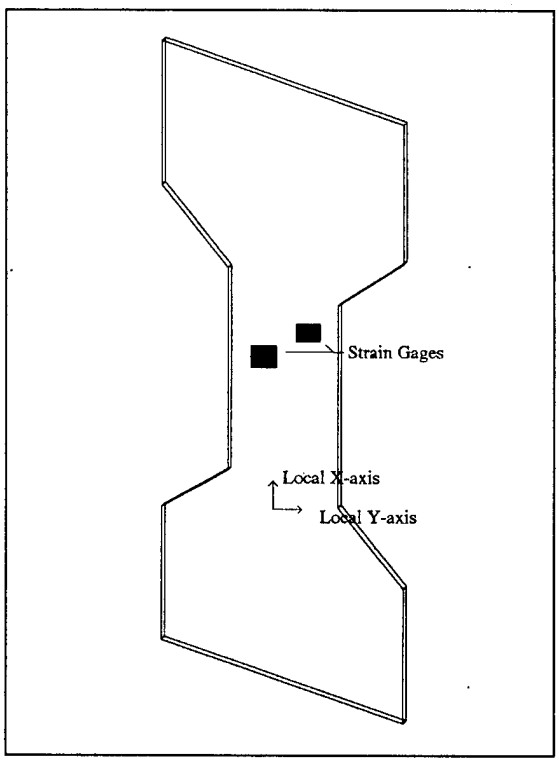


Figure 30. Circuit Board Test Sample

The samples were tested using a MTS Universal Testing Machine- Model 810 at lab facilities at NPS, with the assistance of Jim Scholfield. The machine has a range of 0 to 5000 pounds.

Two strain gages were mounted on each sample, in the test section area. One gage measured axial strain while the other measured transverse strain. The axial direction was taken to be the X- axis of the sample.

The strain gages were Micro Measurements strain gages, Model CEA-13-250-UN-350. Table 15 lists their parameters.

Gage factor	2120 +/-0.5%
Ω	350.0+/-0.3%
K	(+0.5+/-0.2)%

Table 15. Strain gage performance at 24°C

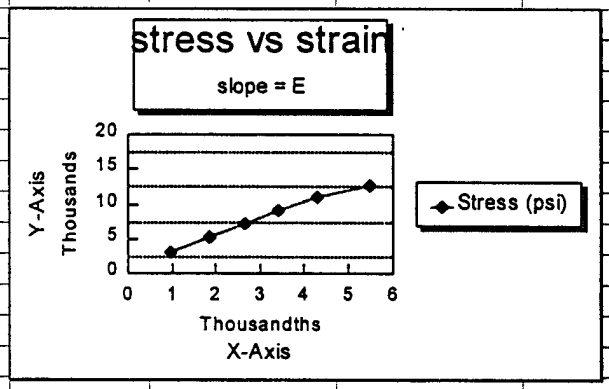
A load was placed on each sample. The corresponding strain in X and Y was recorded. Strain readouts were in microstrain. The load was stepped up incrementally on both samples until the material failed. The microstrains recorded at each load for each sample are shown on the accompanying spread sheet. The spreadsheet was done on Lotus 1-2-3 software. Using the cross sectional area of each sample, the stress due to each load was calculated and stress vs. strain was plotted. The slope of this graph was the modulus of elasticity. (The plots are also shown on the spread sheet.) The slopes (modulus of elasticity) are highlighted. Two linear regressions were done on each sample to determine slope. The first regression used all points on the stress-strain curve. The second regression did not use those points that appeared to be past the elastic limit. This was determined by examining the graph and observing where the slope began to change. All values were averaged to arrive at one value for modulus of elasticity.

A plot was made of X strain vs. Y strain to determine Poisson's Ratio. This plot for each sample is included in the spread sheet. A linear regression for each plot was performed where the slope represents Poisson's ratio. The values from each sample were averaged to produce the value used in this report. Table 16 shows the experimental results compared to the general range of values for these properties.

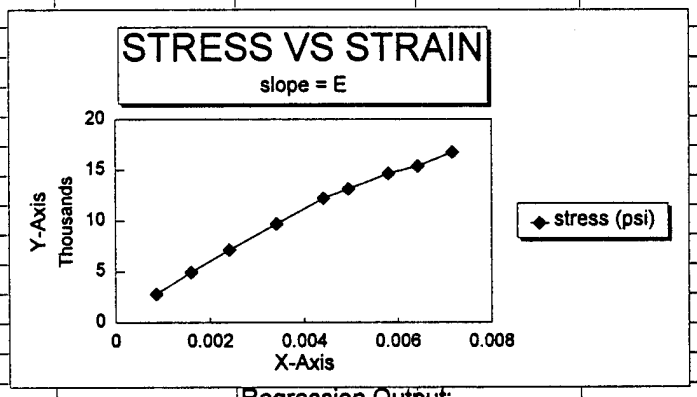
	Experimental Value	General Range
Modulus of Elasticity (psi)	2.33×10^6	$2\text{-}3 \times 10^6$
Poisson's Ratio	0.12	0.12

Table 16. Material Properties

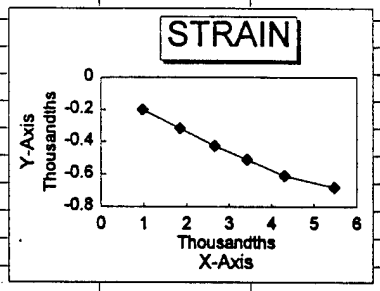
	A	B	C	D	E	F
1						
2		**MATERIAL PROPERTIES TEST ON ' BLUE' CIRCUITBOARD SAMPLE**				
3						
4		Cross sectional area (in^2)			0.0906	
5						
6		load(yy)-lb	load(xx)-lb	YY-(microstrain	XX-microstrai	Stress (psi)
7		267	267	-2.0000E-04	9.700E-04	2947.019868
8		460	470	-3.1600E-04	1.8460E-03	5077.262693
9		650	640	-4.2600E-04	2.6630E-03	7174.392936
10		807	807	-5.0900E-04	3.4210E-03	8907.284768
11		982	982	-6.0800E-04	4.3070E-03	10838.8521
12		1150	1168	-6.8000E-04	5.4730E-03	12693.15673
13		1380	FAILURE			15231.78808
14						
15						
16						
17						
18						
19						
20						
21						
22						
23						
24						
25						
26						
27						
28						
29						
30						
31			Regression Output:			
32		Constant			1097.38336	y intercept
33		Std Err of Y Est			347.836258	
34		R Squared			0.99262736	
35		No. of Observations			6	
36		Degrees of Freedom			4	
37						
38		X Coefficient(s)		**2.20E+06**	**slope=E(psi)**	
39		Std Err of Coef.		94702.93651		
40						
41		recalculate, discarding "bad terms"				
42			**Regression Output:**			
43		Constant			708.84862	
44		Std Err of Y Est			114.557849	
45		R Squared			0.99897813	
46		No. of Observations			5	
47		Degrees of Freedom			3	
48						
49		X Coefficient(s)		2.38E+06	**slope=E(psi)**	
50		Std Err of Coef.		43902.83703		
51		**Average Modulus of Elasticity =**			**2.29E+06**	
52						

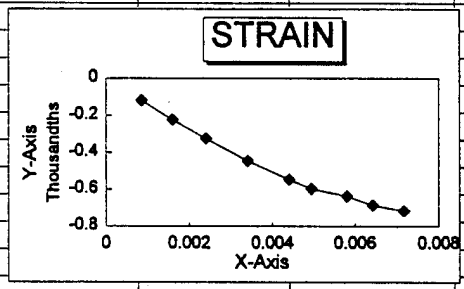


	A	B	C	D	E	F	G
1							
2		**MATERIAL PROPERTIES TEST ON ' ORANGE' CIRCUITBOARD SAMPLE**					
3							
4		Cross sectional area (in^2)			0.083		
5							
6		load(yy)-lb	load(xx)-lb	YY-(microstrain	XX-microstrain	Stress (psi)	
7		235	232	-1.1800E-04	8.5700E-04	2795.181	
8		410	410	-2.2300E-04	1.6000E-03	4939.759	
9		588	592	-3.2300E-04	2.4030E-03	7132.53	
10		809	804	-4.4500E-04	3.4070E-03	9686.747	
11		998	1013	-5.4700E-04	4.4070E-03	12204.82	
12		1100	1089	-5.9700E-04	4.9440E-03	13120.48	
13		1194	1215	-6.3700E-04	5.8000E-03	14638.55	
14		1290	1277	-6.8600E-04	6.4200E-03	15385.54	
15		1379	1390	-7.1700E-04	7.1600E-03	16746.99	
16							
17							
18							
19							
20							
21							
22							
23							
24							
25							
26							
27							
28							
29							
30							
31				Regression Output:			
32			Constant			1640.431	y-intercept
33			Std Err of Y Est			613.0249	
34			R Squared			0.986268	
35			No. of Observations			9	
36			Degrees of Freedom			7	
37							
38			X Coefficient(s)		**2.21E+06**	**slope=E**	
39			Std Err of Coef.		98709.9697		
40							
41				Regression Output:			
42			Constant			832.5183	
43			Std Err of Y Est			238.4079	
44			R Squared			0.997273	
45			No. of Observations			6	
46			Degrees of Freedom			4	
47			X Coefficient(s)		**2.55E+06**	**slope=E**	
48			Std Err of Coef.		66613.6832		
49							
50					**average E=**	**2.38E+06**	



	A	B	C	D	E	F	G
1			DETERMINATION OF POISSON'S RATIO				
2		XX-microstrai	YY-(microstrain)				
3		9.700E-04	-2.0000E-04				
4		1.8460E-03	-3.1600E-04				
5		2.6630E-03	-4.2600E-04				
6		3.4210E-03	-5.0900E-04				
7		4.3070E-03	-6.0800E-04				
8		5.4730E-03	-6.8000E-04				
9							
10							
11							
12							
13							
14		Regression Output:					
15	Constant			-7.9982E-05			
16	Std Err of Y Est			7.1822E-06			
17	R Squared			0.998091695			
18	No. of Observations			4			
19	Degrees of Freedom			2			
20							
21	X Coefficient(s)		-0.127	SLOPE = NU		0.000E+00	
22	Std Err of Coef.		0.003929384				
23							
24							
25		XX-microstrai	YY-(microstrain)				
26		8.5700E-04	-1.1800E-04				
27		1.6000E-03	-2.2300E-04				
28		2.4030E-03	-3.2300E-04				
29		3.4070E-03	-4.4500E-04				
30		4.4070E-03	-5.4700E-04				
31		4.9440E-03	-5.9700E-04				
32		5.8000E-03	-6.3700E-04				
33		6.4200E-03	-6.8600E-04				
34		7.1600E-03	-7.1700E-04				
35							
36							
37			Regression Output:				
38		Constant			-3.236E-05		
39		Std Err of Y Est			0.00001326		
40		R Squared			0.99599813		
41		No. of Observations			6		
42		Degrees of Freedom			4		
43							
44		X Coefficient(s)		-0.117	SLOPE= NU		
45		Std Err of Coef.		0.003703701			
46							
47						AVERAGE NU	
48						-0.122	





APPENDIX C. CLASSICAL PLATE THEORY DEFLECTION

As another means to verify plate deflection, the procedure outlined here was followed [Ref. 9]. This method was used on the case of the circuit board without a stiffener and four sides simply supported. The key equation is

$$\nabla^4 w = \frac{q}{D} \tag{C.1}$$

where

∇ is the del operator

w = deflection

q = distributed load

D = plate stiffness factor

As with the Rayleigh method discussed in the text, a form for deflection is assumed. As before, it is a double sine series summation.

$$W(x,y) = \Sigma\Sigma W_{mn} \sin(\frac{m\pi x}{a})\sin(\frac{n\pi y}{b}) \tag{C.2}$$

The coefficients, W_{mn} are unknown and must be solved for. A form for the distributed load, q, is also assumed, and takes the same form.

$$q = \Sigma\Sigma q_{mn} \sin(\frac{m\pi x}{a})\sin(\frac{n\pi y}{b}) \tag{C.3}$$

The coefficients here, q_{mn} are also unknown. They are found using Fourier analysis. Both sides of the equation are multiplied by

$$\sin(\frac{r\pi x}{a})\sin(\frac{s\pi y}{b}) \tag{C.4}$$

and integrated from -a to a. The dimensions of the circuit board are represented by 'a' and 'b'. Due to the orthogonality property of the sine function, all values drop out except where m=r and n=s. The result gives the value of the coefficients.

$$q_{mn} = \frac{16q_0}{mn\pi^2} \tag{C.5}$$

This value is placed into equation (C.3). It and equation (C.2) are substituted into equation (C.1). Like coefficients of the sine functions on both sides are compared, giving

$$W_{mn}\left[\left(\frac{n\pi}{b}\right)^2 + \left(\frac{m\pi}{a}\right)^2\right]^2 = \frac{16q_0}{Dmn\pi^2} \tag{C.6}$$

This is solved for W_{mn} and summed over odd m and n.

A MATLAB program was written to plot W(x,y) for the logic and switch boards, and is contained in this appendix. Figure 31 shows a MATLAB plot for the logic board.

DEFLECT.M

```
E= 1.61e10 ;            %modulus of elasticity, Pa
nu=0.12;
t=0.001588;             % thickness, meters
D=(E*t^3)/(12*(1-nu^2))% stiffness
rho=3.37;               %density, grams/cm^3
rho1=rho*100^3/1000     %density, kg/m^3
a=0.2032;               %width, meters
b=0.2286;               %length, meters
A=a*b;                  %area
G=-10;                  %acceleration, G force
grav=9.81;              %gravity, meters/sec^2
q0=rho1*t*G*grav        %loading; Pascals
format short e
xnum=7;                 %number of points on board x and y axis
ynum=7;

W=zeros(xnum,ynum)
for m=1:2:9
m;
        for n=1:2:9
        n;
        coef=(16*q0/[D*m*n*pi^2*[((n*pi/b)^2)+((m*pi/a)^2)]^2]);  %
series coefficients
                for i=1:xnum
                        for j=1:ynum
                        x(i)=(i-1)*a/(xnum-1);
                        y(j)=(j-1)*b/(ynum-1);
                        W(i,j)=coef*sin(m*pi*x(i)/a)*sin(n*pi*y(j)/
b)+W(i,j);
                        end
                end

        end
end
W=100/2.54*W     %convert from meters to inches

mesh(y,x,W)
title('Logic Board Deflection (inches)')
```

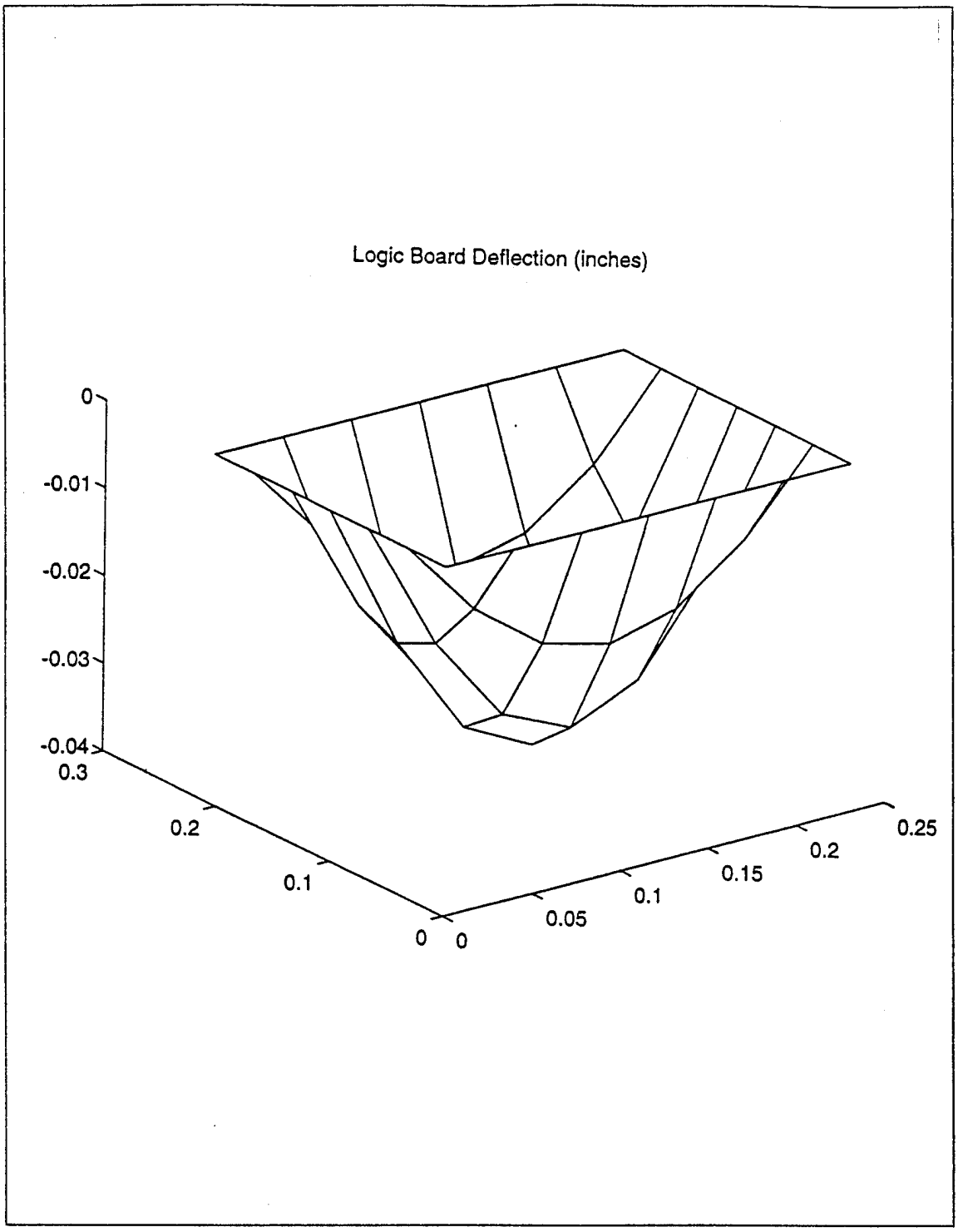


Figure 31. Plate Deflection From Classical Plate Theory

APPENDIX D. NATURAL FREQUENCY (NO STIFFENER)

The natural frequency of the circuit boards in the case of all sides simply supported and the case of two sides simply supported and two sides clamped are discussed in the text. The spreadsheets used to calculate these frequencies are included here.

The calculations are done in both English units and SI units. This is because the measurements were done in English units, and most of the engineering being done on PANSAT is also in English units. However most people are more familiar with SI units, as they are more universal and easier to work with.

The equations for the two cases mentioned are repeated here for convenience.

All edges simply supported:

$$f_n = \frac{\pi}{2}\sqrt{\frac{D}{\rho}}\left(\frac{1}{a^2}+\frac{1}{b^2}\right) \tag{D.1}$$

and for clamped sides:

$$f_n = \frac{\pi}{3.46}\left[\frac{D}{\rho}\left(\frac{16}{a^4}+\frac{8}{a^2b^2}+\frac{3}{b^4}\right)\right]^{1/2} \tag{D.2}$$

D is the plate stiffness and is given by

$$D = \frac{Eh^3}{(12(1-\mu^2))} \tag{D.3}$$

ρ is mass per unit area. This value can be determined by dividing the mass of the board by its area, or multiplying the density of the board by its thickness. In the first iterations of the design the exact weight of the board was not known. As an approximation the density of the material was used with the board thickness to come up with the value used in the spreadsheet.

The values for modulus of elasticity and Poisson's ratio which were experimentally obtained are shown on the spread sheet as well. These numbers were used to determine

D. The spread sheet shows the values obtained for frequency and deflection. The space shuttle longitudinal limit load is 11 G's. This value is used for G_{in}.

A	A	B	C	D	E	F	G
1			LOGIC BOARD VIBRATION ANALYSIS				
2	rho=mass/area=density*thickness						
3	BOARD DIMENSIONS AND PROPERTIES					conversion factors	
4		inches	centimeters	meters			
5	a=length	8.00	20.320	0.2032		inches to cm=	2.54
6	b=width	9.00	22.860	0.2286		psi to Pa=	6.895E+03
7	thickness	0.0625	0.1588	0.001588			
8			(g/cm^3)				
9	density		3.37				
10		(psi)	(Pa)				
11	E (modulus)	2.33E+06	1.61E+10				
12							
13	nu	0.12					
14	stiffness(D)	5.4369	N-M				
15		(g/cm^2)	(kg/m^2)				
16	rho	0.535	5.350				
17							
18				NATURAL FREQUENCY (Hz)			
19							
20	4 SIDES SS		2 SIDES SS + 2 S	DES CL	Fn FOR PCB WITH CARDLOKS		
21	68.65	(Fs)	109.04	(Ff)	108.69	(Fn)	
22							
23							
24	Check each subsection (due to stiffener)						
25							
26	159.56	(Fs)	187.12	(Ff)	184.78	(Fn)	
27							
28	CHECK DEFLECTION (inches)						
29	Gin (g's)	11.00					
30							
31	4 SIDES SS		2 SIDES SS + 2 S	DES CL	Fn FOR PCB WITH CARDLOKS		
32	0.1895		0.0947		0.0951		
33							
34							
35	Check each subsection (due to stiffener)						
36							
37	0.0535		0.0421		0.0429		

A	A	B	C	D	E	F	G
1			SWITCH BOARD VIBRATION ANALYSIS				
2	rho=mass/area=density*thickness						
3	BOARD DIMENSIONS AND PROPERTIES					conversion factors	
4		inches	centimeters	meters			
5	a=length	8.00	20.320	0.2032		inches to cm=	2.54
6	b=width	9.00	22.860	0.2286		psi to Pa=	6.895E+03
7	thickness	0.0625	0.1588	0.001588			
8			(g/cm^3)				
9	density		4.64				
10		(psi)	(Pa)				
11	E (modulus)	2.33E+06	1.61E+10				
12							
13	nu	0.12					
14	stiffness(D)	5.4369	N-M				
15		(g/cm^2)	(kg/m^2)				
16	rho	0.737	7.366				
17							
18				NATURAL FREQUENCY (Hz)			
19							
20	4 SIDES SS		2 SIDES SS+2 S	DES CL		Fn FOR PCB WITH CARD LOKS	
21	58.51	(Fs)	92.93	(Ff)	93.16	(Fn)	
22							
23							
24	Check each subsection (due to stiffener)						
25							
26	135.98	(Fs)	159.47	(Ff)	158.10	(Fn)	
27							
28	CHECK DEFLECTION (Inches)						
29	Gin (g's)	11.00					
30							
31	4 SIDES SS		2 SIDES SS+2 S	DES CL		Fn FOR PCB WITH CARD LOKS	
32	0.2409		0.1203		0.1199		
33							
34							
35	Check each subsection (due to stiffener)						
36							
37	0.0680		0.0535		0.0542		

APPENDIX E. WEIGHTED STIFFNESS

The use of a stiffener modifies the equations for natural frequency as indicated in the text, by changing the stiffness factor so it is no longer isotropic. D is now represented by D_x, D_{xy}, D_y. This appendix shows the calculations performed to obtain their values.

To determine D_x, the new centroid of the board with the stiffener must be determined. The cross sectional view of the board and stiffener are shown in Figure 13.

The new centroid is determined using the Lotus spread sheet attached. Column 4 is the distance from the origin of the coordinate system, which is taken to be the bottom of the circuit board, to the centroid of each item, in the Z direction. Column 7 is the moment of inertia for each item. Column 6 is divided by column 5 to produce the centroid of the board and stiffener. Column 9 is the distance in the Z direction from the centroid of each part to the centroid of the whole.

The bending stiffness is then determined by summing columns 8 and 11 for both items. This gives EI which is used to determine D_x .

$$D_x = \frac{EI}{d} \tag{E.1}$$

D_{xy} is given by

$$D_{xy} = G_e J_e + \frac{G_r J_r}{2d} \tag{E.2}$$

where

$$G_e = \frac{E}{2(1+\nu)} \quad = \text{shear modulus of circuit board.} \tag{E.3}$$

$J_e = \frac{t^3}{3}$ = torsional stiffness of circuit board. t = thickness

G_r = shear modulus of stiffener

J_r = torsional stiffness of stiffener

These values are calculated on the spread sheet as shown, to yield D_x and D_{xy} .

A	A	B	C	D	E	F	G
38			ANALYZE LOGIC BOARD WITH STIFFENER				
39							
40	modify simply supported equation to: Fs=(pi/2)*sqrt[(1/rho)(Dx/a^4+4Dxy/a^2b^2+Dy/b^4)]						
41							
42	modify 2 clamped, 2 supported eqn to: Ff=(pi/3.46)sqrt[(1/rho)(16Dx/a^4+16Dxy/a^2b^2+3Dy/b^4)]						
43							
44				STIFFENER			
45							
46					ALUMINUM	STEEL	POLYIMIDE
47	Height (in)=	0.30		E(psi)=	9.90E+06	2.9E+07	2.33E+06
48	height (m)=	0.0076		E(Pa)	6.83E+10	2.00E+11	1.61E+10
49	length(in)=	8.0000		Gr(lb/in^2)=	4.00E+06		
50	length(m)=	0.2032		Gr(Pa)=	2.76E+10		
51	thickness(")	0.1250		Jr= (m^4)	3.43E-11		
52	thickness(m)	0.0032					
53	bonding_eff	0.7500	assuming75% efficiency (from .125)				
54	equiv thick(m	0.002381					
55	equiv thick(")	0.0938					
56							
57	Dx=EI/d						
58	EI = Material weighted stiffness						
59	d= rib spacing						
60	Dxy=GeJe+GrJr/2d						
61	Ge=E/(2(1+nu))		shear modulus of circuit board			7.16E+09	Pa
62	Je=t^3/3		torsional stiffness of circuit board, t=PCB thickness			1.33E-09	m^4
63	Gr=shear modulus of stiffener						
64	Jr=1/3*(stiff ht)(stiff thick)^3						
65	Dy= D from no stiffener case						
66							
67	NEED TO CALCULATE WEIGHTED STIFFNESS						
68							
69	**Item**	**Area(m^2)**	**E(Pa)**	**Z(dist to cent)(m)**	**AE(N)**	**AEZ(N-m)**	
70	PCB	0.000363	1.61E+10	0.00079	5.830E+06	4.628E+03	
71	stiffener	0.000018	6.83E+10	0.00540	1.239E+06	6.685E+03	
72							
73	total				7.069E+06	1.131E+04	
74							
75				**part cent to**			
76	**Item**	**Io=(bh^3)/12**	**Elo**	**body cent(m)**	**c^2**	**AEc^2**	
77	PCB	7.621E-11	1.224	0.00081	6.51E-07	3.794	
78	stiffener	8.780E-11	5.993	0.00380	1.44E-05	17.857	
79							
80	total		7.217			21.651	
81							
82	centroid of board and stiffener=sum of AEZ/AE=				0.00160	in meters in Z direction	
83	bending stiffness=EI=Elo+AEc^2=			28.868	N-m^2		
84							
85	then				which leads to:		
86	Dx=EI/d=	126.28	N-m		Fs=	212.160	
87	Dxy=	11.62	N-m		Ff=	443.648	
88	Dy=	5.44	N-m				
89					So Fn for stiffened board =		379.051
90		Gin (g's) =	11.00				
91	estimate transmissibility as Q=1*sqrt(Fn)=				19.4692		
92	estimate deflection as delta=9.8*Gin*Q/Fn^2=				0.0146	inches see p165	
93					0.0349	four simply supported	
94							

	A	B	C	D	E	F	G
38			ANALYZE LOGIC BOARD WITH STIFFENER				
39							
40	modify simply supported equation to: Fs=(pi/2)*sqrt[(1/rho)(Dx/a^4+4Dxy/a^2b^2+Dy/b^4)]						
41							
42	modify 2 clamped, 2 supported eqn to: Ff=(pi/3.46)sqrt[(1/rho)(16Dx/a^4+16Dxy/a^2b^2+3Dy/b^4)]						
43							
44				STIFFENER			
45							
46					ALUMINUM	STEEL	POLYIMIDE
47	Height (in)=	0.30		E(psi)=	9.90E+06	2.9E+07	2.33E+06
48	height (m)=	0.0076		E(Pa)	6.83E+10	2.00E+11	1.61E+10
49	length(in)=	8.0000		Gr(lb/in^2)=	4.00E+06		
50	length(m)=	0.2032		Gr(Pa)=	2.76E+10		
51	thickness(")	0.2000		Jr= (m^4)	1.40E-10		
52	thickness(m)	0.0051					
53	bonding eff	0.7500	assuming75% efficiency (from .125)				
54	equiv thick(m	0.003810					
55	equiv thick(")	0.1500					
56							
57	Dx=EI/d						
58	EI = Material weighted stiffness						
59	d= rib spacing						
60	Dxy=GeJe+GrJr/2d						
61	Ge=E/(2(1+nu))		shear modulus of circuit board			7.16E+09	Pa
62	Je=t^3/3		torsional stiffness of circuit board, t=PCB thickness			1.33E-09	m^4
63	Gr=shear modulus of stiffener						
64	Jr=1/3*(stiff ht)(stiff thick)^3						
65	Dy= D from no stiffener case						
66							
67	NEED TO CALCULATE WEIGHTED STIFFNESS						
68							
69	**Item**	**Area(m^2)**	**E(Pa)**	**Z(dist to cent)(m)**	**AE(N)**	**AEZ(N-m)**	
70	PCB	0.000363	1.61E+10	0.00079	5.830E+06	4.628E+03	
71	stiffener	0.000029	6.83E+10	0.00540	1.982E+06	1.070E+04	
72							
73	total				7.812E+06	1.532E+04	
74							
75				**part cent to**			
76	**Item**	**Io=(bh^3)/12**	**Elo**	**body cent(m)**	**c^2**	**AEc^2**	
77	PCB	7.621E-11	1.224	0.00117	1.36E-06	7.952	
78	stiffener	1.405E-10	9.589	0.00344	1.18E-05	23.394	
79							
80	total		10.813			31.346	
81							
82	centroid of board and stiffener=sum of AEZ/AE=				0.00196	in meters in Z	direction
83	bending stiffness=EI=Elo+AEc^2=			42.159	N-m^2		
84							
85	then				which leads to:		
86	Dx=EI/d=	184.42	N-m		Fs=	257.325	
87	Dxy=	18.02	N-m		Ff=	536.866	
88	Dy=	5.44	N-m				
89					So Fn for stiffened board =		441.424
90		Gin (g's) =	11.00				
91	estimate transmissibility as Q=1*sqrt(Fn)=				21.0101		
92	estimate deflection as delta=9.8*Gin*Q/Fn^2=				0.0116	inches see p165	
93					0.0261	four simply supported	
94							

A	A	B	C	D	E	F	G
38			**ANALYZE LOGIC BOARD WITH STIFFENER**				
39							
40	modify simply supported equation to: Fs=(pi/2)*sqrt[(1/rho)(Dx/a^4+4Dxy/a^2b^2+Dy/b^4)]						
41							
42	modify 2 clamped, 2 supported eqn to: Ff=(pi/3.46)sqrt[(1/rho)(16Dx/a^4+16Dxy/a^2b^2+3Dy/b^4)]						
43							
44				**STIFFENER**			
45							
46					ALUMINUM	STEEL	POLYIMIDE
47	Height (in)=	0.40		E(psi)=	9.90E+06	2.9E+07	2.33E+06
48	height (m)=	0.0102		E(Pa)	6.83E+10	2.00E+11	1.61E+10
49	length(in)=	8.0000		Gr(lb/in^2)=	4.00E+06		
50	length(m)=	0.2032		Gr(Pa)=	2.76E+10		
51	thickness(")	0.1250		Jr= (m^4)	4.57E-11		
52	thickness(m)	0.0032					
53	bonding eff	0.7500	assuming75% efficiency (from .125)				
54	equiv thick(m	0.002381					
55	equiv thick(")	0.0938					
56							
57	Dx=EI/d						
58	EI = Material weighted stiffness						
59	d= rib spacing						
60	Dxy=GeJe+GrJr/2d						
61	Ge=E/(2(1+nu))		shear modulus of circuit board			7.16E+09	Pa
62	Je=t^3/3		torsional stiffness of circuit board, t=PCB thickness			1.33E-09	m^4
63	Gr=shear modulus of stiffener						
64	Jr=1/3*(stiff ht)(stiff thick)^3						
65	Dy= D from no stiffener case						
66							
67	NEED TO CALCULATE WEIGHTED STIFENESS						
68							
69	**Item**	**Area(m^2)**	**E(Pa)**	**Z(dist to cent)(m)**	**AE(N)**	**AEZ(N-m)**	
70	PCB	0.000363	1.61E+10	0.00079	5.830E+06	4.628E+03	
71	stiffener	0.000024	6.83E+10	0.00667	1.651E+06	1.101E+04	
72							
73	total				7.481E+06	1.564E+04	
74							
75				**part cent to**			
76	**Item**	**Io=(bh^3)/12**	**Elo**	**body cent(m)**	**c^2**	**AEc^2**	
77	PCB	7.621E-11	1.224	0.00130	1.68E-06	9.800	
78	stiffener	2.081E-10	14.206	0.00458	2.10E-05	34.598	
79							
80	total		15.430			44.399	
81							
82	centroid of board and stiffener=sum of AEZ/AE=				0.00209	in meters in Z direction	
83	bending stiffness=EI=Elo+AEc^2=			59.828	N-m^2		
84							
85	then				which leads to:		
86	Dx=EI/d=	261.72	N-m		Fs=	286.774	
87	Dxy=	12.31	N-m		Ff=	627.278	
88	Dy=	5.44	N-m				
89					So Fn for stiffened board =		493.343
90		Gin (g's) =	11.00				
91	estimate transmissibility as Q=1*sqrt(Fn)=				22.2113		
92	estimate deflection as delta=9.8*Gin*Q/Fn^2=				0.0098	inches see p165	
93					0.0222	four simply supported	
94							

	A	B	C	D	E	F	G
38			ANALYZE SWITCH BOARD WITH STIFFENER				
39							
40	modify simply supported equation to: Fs=(pi/2)*sqrt[(1/rho)(Dx/a^4+4Dxy/a^2b^2+Dy/b^4)]						
41							
42	modify 2 clamped, 2 supported eqn to: Ff=(pi/3.46)sqrt[(1/rho)(16Dx/a^4+16Dxy/a^2b^2+3Dy/b^4)]						
43							
44				STIFFENER			
45							
46					ALUMINUM	STEEL	POLYIMIDE
47	Height (in)=	0.30		E(psi)=	9.90E+06	2.9E+07	2.33E+06
48	height (m)=	0.0076		E(Pa)	6.83E+10	2.00E+11	1.61E+10
49	length(in)=	8.0000		Gr(lb/in^2)=	4.00E+06		
50	length(m)=	0.2032		Gr(Pa)=	2.76E+10		
51	thickness(")	0.1250		Jr= (m^4)	3.43E-11		
52	thickness(m)	0.0032					
53	bonding eff	0.7500	assuming75% efficiency (from .125)				
54	equiv thick(m	0.002381					
55	equiv thick(")	0.0938					
56							
57	Dx=EI/d						
58	EI = Material weighted stiffness						
59	d= rib spacing						
60	Dxy=GeJe+GrJr/2d						
61	Ge=E/(2(1+nu))		shear modulus of circuit board			7.16E+09	Pa
62	Je=t^3/3		torsional stiffness of circuit board, t=PCB thickness			1.33E-09	m^4
63	Gr=shear modulus of stiffener						
64	Jr=1/3*(stiff ht)(stiff thick)^3						
65	Dy= D from no stiffener case						
66							
67	NEED TO CALCULATE WEIGHTED STIFFNESS						
68							
69	**Item**	**Area(m^2)**	**E(Pa)**	**Z(dist to cent)(m)**	**AE(N)**	**AEZ(N-m)**	
70	PCB	0.000363	1.61E+10	0.00079	5.830E+06	4.628E+03	
71	stiffener	0.000018	6.83E+10	0.00540	1.239E+06	6.685E+03	
72							
73	total				7.069E+06	1.131E+04	
74							
75				**part cent to**			
76	**Item**	**Io=(bh^3)/12**	**Elo**	**body cent(m)**	**c^2**	**AEc^2**	
77	PCB	7.621E-11	1.224	0.00081	6.51E-07	3.794	
78	stiffener	8.780E-11	5.993	0.00380	1.44E-05	17.857	
79							
80	total		7.217			21.651	
81							
82	centroid of board and stiffener=sum of AEZ/AE=				0.00160	in meters in Z direction	
83	bending stiffness=EI=Elo+AEc^2=			28.868	N-m^2		
84							
85	then				which leads to:		
86	Dx=EI/d=	126.28	N-m		Fs=	180.808	
87	Dxy=	11.62	N-m		Ff=	378.090	
88	Dy=	5.44	N-m				
89					So Fn for stiffened board =		332.268
90		Gin (g's) =	11.00				
91	estimate transmissibility as Q=1*sqrt(Fn)=				18.2282		
92	estimate deflection as delta=9.8*Gin*Q/Fn^2=				0.0178	inches see p165	
93					0.0443	four simply supported	
94							

	A	B	C	D	E	F	G
38			ANALYZE SWITCH BOARD WITH STIFFENER				
39							
40	modify simply supported equation to: Fs=(pi/2)*sqrt[(1/rho)(Dx/a^4+4Dxy/a^2b^2+Dy/b^4)]						
41							
42	modify 2 clamped, 2 supported eqn to: Ff=(pi/3.46)sqrt[(1/rho)(16Dx/a^4+16Dxy/a^2b^2+3Dy/b^4)]						
43							
44				STIFFENER			
45							
46					ALUMINUM	STEEL	POLYIMIDE
47	Height (in)=	0.30		E(psi)=	9.90E+06	2.9E+07	2.33E+06
48	height (m)=	0.0076		E(Pa)	6.83E+10	2.00E+11	1.61E+10
49	length(in)=	8.0000		Gr(lb/in^2)=	4.00E+06		
50	length(m)=	0.2032		Gr(Pa)=	2.76E+10		
51	thickness(")	0.2000		Jr= (m^4)	1.40E-10		
52	thickness(m)	0.0051					
53	bonding eff	0.7500	assuming75% efficiency (from .125)				
54	equiv thick(m	0.003810					
55	equiv thick(")	0.1500					
56							
57	Dx=EI/d						
58	EI = Material weighted stiffness						
59	d= rib spacing						
60	Dxy=GeJe+GrJr/2d						
61	Ge=E/(2(1+nu))		shear modulus of circuit board			7.16E+09	Pa
62	Je=t^3/3		torsional stiffness of circuit board, t=PCB thickness			1.33E-09	m^4
63	Gr=shear modulus of stiffener						
64	Jr=1/3*(stiff ht)(stiff thick)^3						
65	Dy= D from no stiffener case						
66							
67	NEED TO CALCULATE WEIGHTED STIFFNESS						
68							
69	**Item**	**Area(m^2)**	**E(Pa)**	**Z(dist to cent)(m)**	**AE(N)**	**AEZ(N-m)**	
70	PCB	0.000363	1.61E+10	0.00079	5.830E+06	4.628E+03	
71	stiffener	0.000029	6.83E+10	0.00540	1.982E+06	1.070E+04	
72							
73	total				7.812E+06	1.532E+04	
74							
75				**part cent to**			
76	**Item**	**Io=(bh^3)/12**	**Elo**	**body cent(m)**	**c^2**	**AEc^2**	
77	PCB	7.621E-11	1.224	0.00117	1.36E-06	7.952	
78	stiffener	1.405E-10	9.589	0.00344	1.18E-05	23.394	
79							
80	total		10.813			31.346	
81							
82	centroid of board and stiffener		=sum of AEZ/AE=		0.00196	in meters in Z direction	
83	bending stiffness=EI=Elo+AEc^2=			42.159	N-m^2		
84							
85	then				which leads to:		
86	Dx=EI/d=	184.42	N-m		Fs=	219.299	
87	Dxy=	18.02	N-m		Ff=	457.532	
88	Dy=	5.44	N-m				
89					So Fn for stiffened board =		388.744
90		Gin (g's) =	11.00				
91	estimate transmissibility as Q=1*sqrt(Fn)=				19.7166		
92	estimate deflection as delta=9.8*Gin*Q/Fn^2=				0.0144	inches see p165	
93					0.0332	four simply supported	
94							

A	A	B	C	D	E	F	G
38			ANALYZE SWITCH BOARD WITH STIFFENER				
39							
40	modify simply supported equation to: Fs=(pi/2)*sqrt[(1/rho)(Dx/a^4+4Dxy/a^2b^2+Dy/b^4)]						
41							
42	modify 2 clamped, 2 supported eqn to: Ff=(pi/3.46)sqrt[(1/rho)(16Dx/a^4+16Dxy/a^2b^2+3Dy/b^4)]						
43							
44				STIFFENER			
45							
46					ALUMINUM	STEEL	POLYIMIDE
47	Height (in)=	0.40		E(psi)=	9.90E+06	2.9E+07	2.33E+06
48	height (m)=	0.0102		E(Pa)	6.83E+10	2.00E+11	1.61E+10
49	length(in)=	8.0000		Gr(lb/in^2)=	4.00E+06		
50	length(m)=	0.2032		Gr(Pa)=	2.76E+10		
51	thickness(")	0.1250		Jr= (m^4)	4.57E-11		
52	thickness(m)	0.0032					
53	bonding eff	0.7500	assuming75% efficiency (from .125)				
54	equiv thick(m	0.002381					
55	equiv thick(")	0.0938					
56							
57	Dx=EI/d						
58	EI = Material weighted stiffness						
59	d= rib spacing						
60	Dxy=GeJe+GrJr/2d						
61	Ge=E/(2(1+nu))		shear modulus of circuit board			7.16E+09	Pa
62	Je=t^3/3		torsional stiffness of circuit board, t=PCB thickness			1.33E-09	m^4
63	Gr=shear modulus of stiffener						
64	Jr=1/3*(stiff ht)(stiff thick)^3						
65	Dy= D from no stiffener case						
66							
67	NEED TO CALCULATE WEIGHTED STIFFNESS						
68							
69	**Item**	**Area(m^2)**	**E(Pa)**	**Z(dist to cent)(m)**	**AE(N)**	**AEZ(N-m)**	
70	PCB	0.000363	1.61E+10	0.00079	5.830E+06	4.628E+03	
71	stiffener	0.000024	6.83E+10	0.00667	1.651E+06	1.101E+04	
72							
73	total				7.481E+06	1.564E+04	
74							
75				**part cent to**			
76	**Item**	**Io=(bh^3)/12**	**Elo**	**body cent(m)**	**c^2**	**AEc^2**	
77	PCB	7.621E-11	1.224	0.00130	1.68E-06	9.800	
78	stiffener	2.081E-10	14.206	0.00458	2.10E-05	34.598	
79							
80	total		15.430			44.399	
81							
82	centroid of board and stiffener=sum of AEZ/AE=				0.00209	in meters in Z direction	
83	bending stiffness=EI=Elo+AEc^2=			59.828	N-m^2		
84							
85	then				which leads to:		
86	Dx=EI/d=	261.72	N-m		Fs=	244.397	
87	Dxy=	12.31	N-m		Ff=	534.584	
88	Dy=	5.44	N-m				
89					So Fn for stiffened board =		436.838
90		Gin (g's) =	11.00				
91	estimate transmissibility as Q=1*sqrt(Fn)=				20.9007		
92	estimate deflection as delta=9.8*Gin*Q/Fn^2=				0.0118	inches see p165	
93					0.0282	four simply supported	
94							

APPENDIX F. DETAILED HOUSING DIMENSIONS

This appendix contains figures of each of the four pieces of the EPS housing showing key dimensions. The main body of the housing is symmetric. Figure 32 shows an overview while Figure 33 shows the detail of the right front corner. Figures 34-36 show the other parts of the housing. For the D-connector cutouts locations to the cutouts are given. The actual dimensions for each cutout is given in Appendix A.

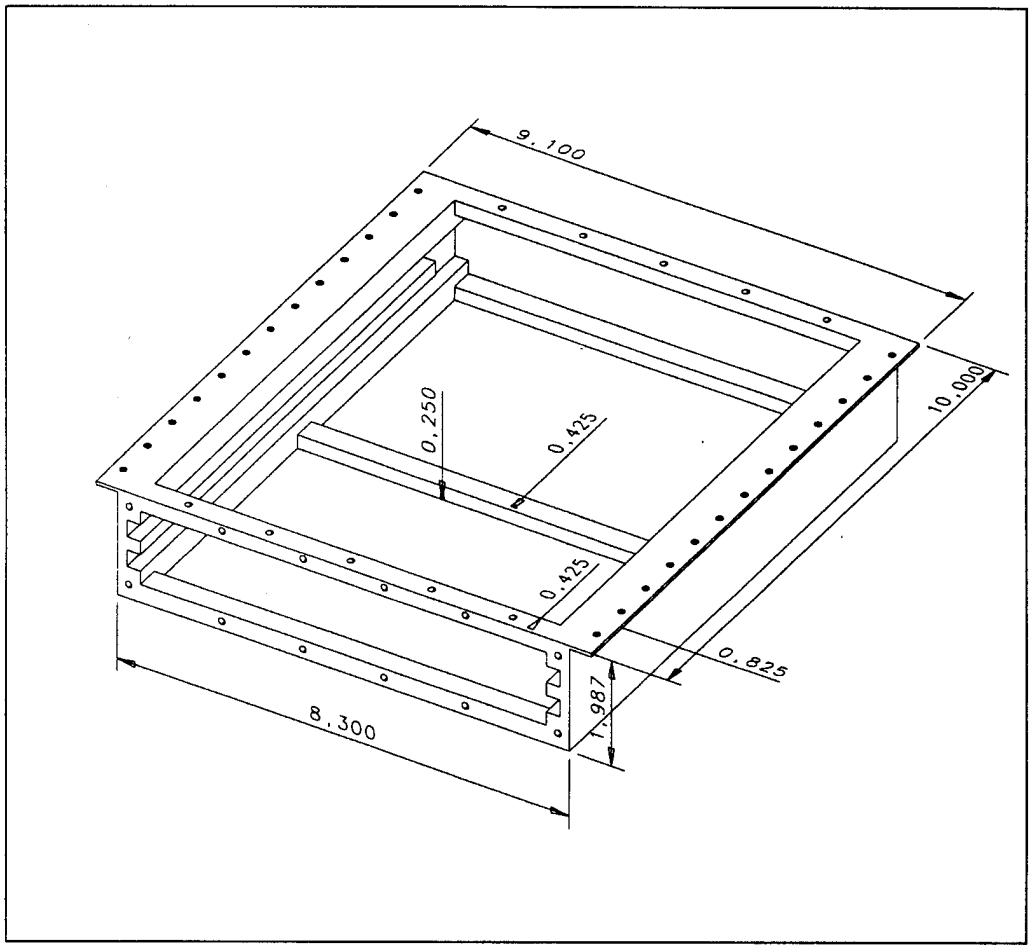


Figure 32. EPS Housing

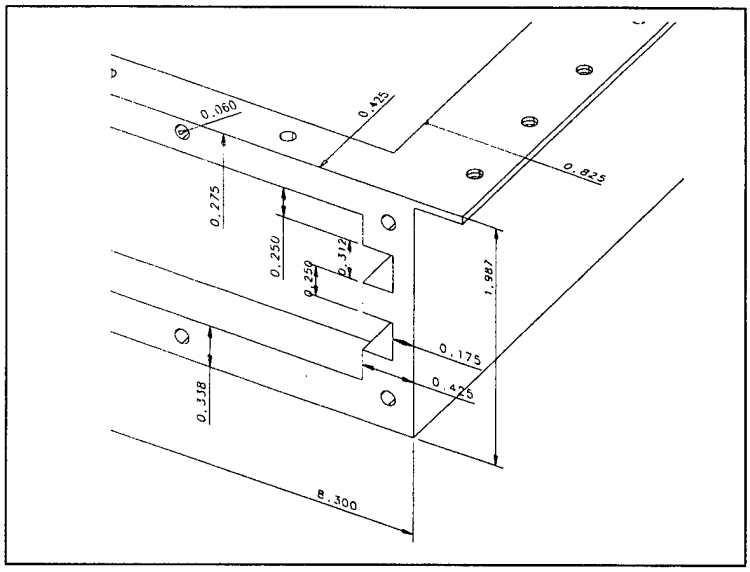


Figure 33. Housing Right Front Corner

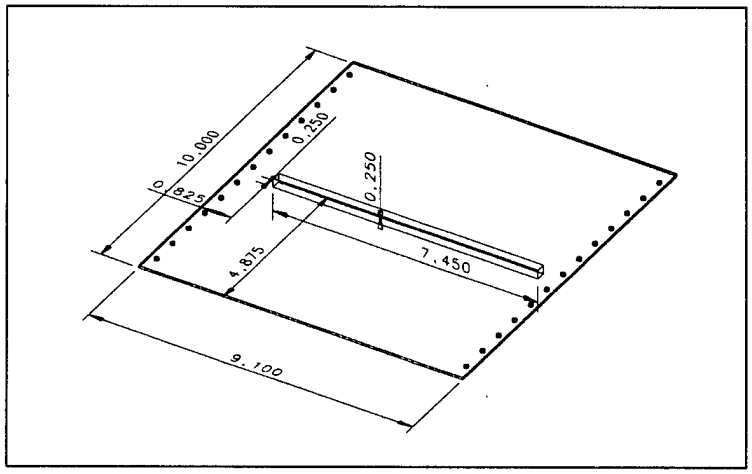


Figure 34. EPS Top Cover

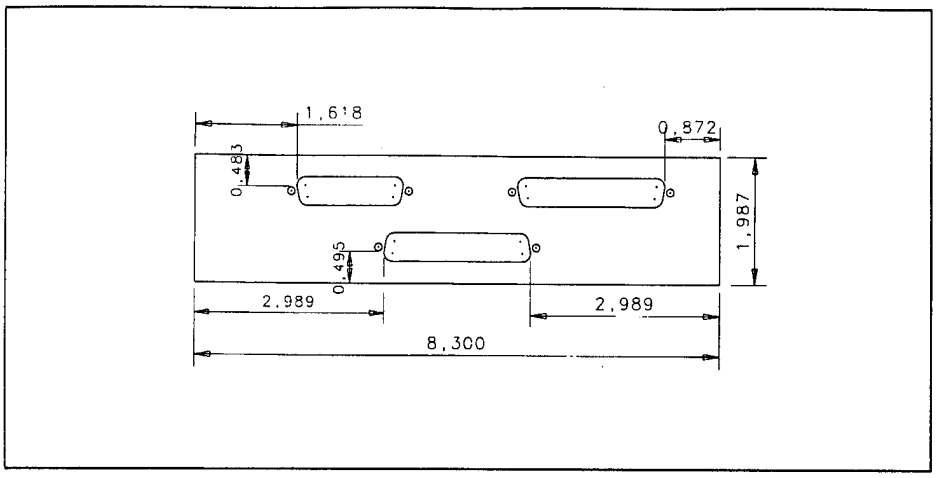


Figure 35. EPS Front Cover

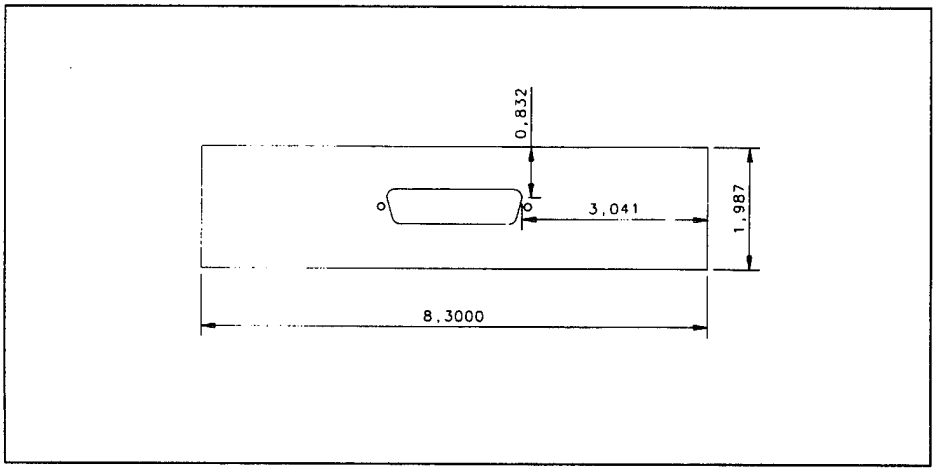


Figure 36. EPS Back Cover

APPENDIX G. NOTES TO I-DEAS USERS

Some difficulties were encountered when making Finite Element Models (FEM) in I-DEAS. They are discussed here for the benefit of future I-DEAS users.

The circuit boards and stiffeners are made of different materials. The two parts become one volume when they are joined. When making the FEM, they must be separated into two volumes so that the mesh has the appropriate properties of each material applied in the right area. Several methods exist for separating the part into two volumes. The I-DEAS on-line help describes these in detail.

The stiffener divided the top surface of the circuit boards into two regions. When the surface is meshed the area under the stiffener is not automatically meshed. This region must be specifically selected so that it may be meshed. In this case elements had to be manually created to ensure a complete model.

As mentioned in Chapter IV, the size of the tetrahedral solid elements used when free meshing a volume is a critical parameter. The housing was meshed using elements 0.8 inches in size. The value obtained for natural frequency was over 5000 Hz. This answer was grossly incorrect, yet no errors are provided by the software to alert the user. Great care must be taken to ensure the correct element size is chosen.

Disk space became an issue in a few instances. In order to overcome the incorrect frequencies mentioned above, a FEM was made of the housing using much smaller size elements. The computer attempted to mesh for over 12 hours, generating over 100,000 nodes, without completing the task. Based on previous experience a model this size would have caused a system crash when a solution was attempted.

The on-line help is very useful. It was able to answer many questions.

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